ARTS IIA Design Analysis

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Final Report

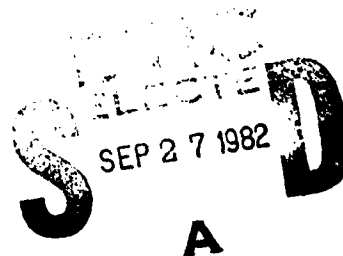This document is available to the U.S. public
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16. Abstract

This report documents the analysis performed by the COMSIS Corporation and SRI International of the proposed design for the ARTS IIA air traffic system for terminal areas with low to medium traffic density. ARTS II will be upgraded to ARTS IIA with the replacement of the LSI-2/20 minicomputer by the LSI-2/40, which is faster and has more memory capacity, and the addition of minimum safe altitude warning (MSAW), conflict alert (CA), a tracker to support these, and a training target generator (TTG). The study addressed the use of semiconductor memory in an air traffic system and the requirement for a battery backup power supply. The algorithms for the enhancements were studied to determine whether the LSI-2/40 has sufficient speed to perform them under traffic and display loads expected in 1990. It is concluded that the replacement computer has the capacity to perform the enhancement functions under maximum target and display load for the expected air traffic environment.

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METRIC CONVERSION FACTORS

Approximate Conversions to Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
in	inches	*2.5	centimeters	cm
ft	feet	30	centimeters	cm
yd	yards	0.9	meters	m
mi	miles	1.6	kilometers	km
		AREA		
in²	square inches	6.5	square centimeters	cm²
ft²	square feet	0.09	square meters	m²
yd²	square yards	0.8	square meters	m²
mi²	square miles	2.6	square kilometers	km²
	acres	0.4	hectares	ha
		MASS (weight)		
oz	ounces	28	grams	g
lb	pounds	0.45	kilograms	kg
	short tons (2000 lb)	0.9	tonnes	t
		VOLUME		
tsp	teaspoons	5	milliliters	ml
Tbsp	tablespoons	15	milliliters	ml
fl oz	fluid ounces	30	milliliters	ml
c	cups	0.24	liters	l
pt	pints	0.47	liters	l
qt	quarts	0.95	liters	l
gal	gallons	3.8	liters	l
ft³	cubic feet	0.03	cubic meters	m³
yd³	cubic yards	0.76	cubic meters	m³
		TEMPERATURE (exact)		
°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

*1 in = 2.54 (exactly). For other exact conversions and more detailed data and tables, see NBS Misc. Publ. 286, Units of Weights and Measures, Price $2.25, SD Catalog No. C13.10:286.

Approximate Conversions from Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
mm	millimeters	0.04	inches	in
cm	centimeters	0.4	inches	in
m	meters	3.3	feet	ft
m	meters	1.1	yards	yd
km	kilometers	0.6	miles	mi
		AREA		
cm²	square centimeters	0.16	square inches	in²
m²	square meters	1.2	square yards	yd²
km²	square kilometers	0.4	square miles	mi²
ha	hectares (10,000 m²)	2.5	acres	
		MASS (weight)		
g	grams	0.035	ounces	oz
kg	kilograms	2.2	pounds	lb
t	tonnes (1000 kg)	1.1	short tons	
		VOLUME		
ml	milliliters	0.03	fluid ounces	fl oz
l	liters	2.1	pints	pt
l	liters	1.06	quarts	qt
l	liters	0.26	gallons	gal
m³	cubic meters	35	cubic feet	ft³
m³	cubic meters	1.3	cubic yards	yd³
		TEMPERATURE (exact)		
°C	Celsius temperature	9/5 (then add 32)	Fahrenheit temperature	°F

°F   -40   0   32   80   98.6   120   160   200   212
      -40   -20   0   20   37   40   60   80   100
°C

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ACRONYMS

ARTS	Automated radar terminal system
APC	Acquisition and processing cabinet
ARTCC	Air Route Traffic Control Center
ASR	Airport surveillance radar
ATCBI	Air traffic control beacon interrogator
BANS	Bright alphanumeric subsystem
BRITE	Bright radar indicator tower equipment
CA	Conflict alert
DDAS	Decoding data acquisition subsystem
DMA	Direct memory addressing
DPS	Data processing subsystem
FAATC	Federal Aviation Administration Technical Center
IFDS	Interfacility data subsystem
IFR	Instrument flight rules
MMU	Memory management unit
MOS	Metallic oxide semiconductor
MSAW	Minimum safe altitude warning
PPI	Plan position indicator
RADS	Radar alphanumeric display subsystem
RAM	Random-access memory
SPI	Special position indicator
TTG	Training target generator
UPS	Uninterruptible power supply

EXECUTIVE SUMMARY

This report presents the results of a study undertaken to analyze the design for the planned ARTS IIA system. The study was performed to resolve questions raised during an earlier project in which the ARTS IIA design was recommended.

The current ARTS II system provides automation for air traffic control at airports that handle traffic of low to medium density. Alphanumeric flight data, presented on PPI radar displays, are time-shared with the normal radar display of primary and beacon targets. Automatic functions performed by ARTS II include identifying new beacon targets, associating those targets with previously entered flight plan data, and selecting a display format for each target on the basis of target status and type and the designated or requested controller display status. Other functions are managing display data, processing flight data or display requests, routing of ARTCC messages, and processing and reducing target input data from the radar beacon decoder.

The planned ARTS IIA system will add the following functions:

- Minimum safe altitude warning (MSAW).

- Conflict alert (CA).

- Alarm notification and presentation to the controller (aural and display data block).

- Training target generator (TTG).

Because its speed and memory size are limited, the current ARTS II computer, a Computer Automation LSI-2/20, cannot perform these additional functions; thus, that computer will be replaced. The

recommended replacement, the LSI-2/40, is upgrade-compatible with the LSI-2/20 and provides approximately twice the speed and much larger memory capability. Hardware replacement and the development of software for the enhancements will be independent activities, thus providing a phased installation approach.

In this study, the following points were considered to ensure the suitability of the LSI-2/40 for ARTS IIA:

- Abilities of various power supplies with an integrated backup battery to provide for retention of the contents of semiconductor memory during power line transients and fluctuations.

- Code transportability between the LSI-2/20 and LSI-2/40.

- Compatibility, performance, and capacity of the LSI-2/40.

- Computer requirements (speed and memory) of the safety enhancements based on air traffic at ARTS II sites in 1990.

All the approaches to solving the problem of semiconductor memory backup involve the use of a rechargeable battery. Computer Automation has not yet designed such backup systems specifically for the memory boards that will be used in ARTS IIA, although they are expected to be available later in 1982. Purchase and testing of an uninterruptible power supply from an independent manufacturer is possible now, although such a unit would not be contained within the existing ARTS APC.

The current code released to the field for 32K ARTS systems is totally compatible with the LSI-2/40. Modification of the code for the 40K version will be necessary to initialize the memory management unit (MMU), which provides an expanded address space, and to maintain MMU status in the event of power failure. These changes are modular and can be easily accomplished at FAATC.

Traffic forecasts for 1990 indicate the requirement for processing 46 tracked targets at the busiest ARTS II site. The LSI-2/40 computer has sufficient speed to provide the safety enhancements under a load of 200 targets and 48 tracks for the maximum 11 displays. Up to 64 tracks can be processed with maximum target load for all but the most highly display-configured systems.

In summary, no major technical problems exist to impede the development of ARTS IIA. All the safety enhancements have already been implemented for ARTS III and need only be restructured for the ARTS IIA computer. Various alternatives are available for the provision of a battery-backup power supply. Finally, the LSI-2/40 computer has the capacity to meet projected air traffic requirements through 1990, and phased hardware installation and software development are feasible.

I INTRODUCTION

The Federal Aviation Administration has been installing the Automated Radar Terminal System II (ARTS II) over the past 5 years to help control air traffic at low- to medium-traffic airports. ARTS II consists of:

- Data processing equipment contained in the acquisition processing cabinet (APC) in the equipment room of the facility.

- One or more radar alphanumeric display subsystems (RADS) in the IFR room.

- A bright alphanumeric subsystem (BANS) to interface with the BRITE displays in the tower cab.

The APC contains the Decoding Data Acquisition Subsystem (DDAS) and the computer. DDAS receives radar video responses from both broadband airport surveillance radars (ASRs) and air traffic control beacon interrogators (ATCBIs). Radar video (both primary and beacon) is presented on plan position indicator (PPI) displays. In addition, the computer presents a single symbol for each beacon-equipped aircraft and a two-line display tag containing the identity and altitude of the aircraft. Other features include SPI and emergency flagging; handoff procedure; automatic data block acquisition and termination; preview, tab, and system display areas; and interfacility communication.

To increase the safety benefits of the ARTS II system, the FAA plans to install some of the safety functions and features now operational on ARTS III. These enhancements include conflict alert (CA), minimum safe altitude warning (MSAW), and training capability through a training target generator (TTG). In addition, MSAW and CA require a beacon tracking routine, a display enhancement that allows display of three lines in each full data block, and an external aural alarm. This enhanced ARTS II system is designated ARTS IIA.

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The ARTS II computer, a Computer Automation LSI-2/20, is already heavily loaded for existing functions under dense traffic and maximum configuration conditions. Although this computer adequately performs the currently required functions, its memory and processing speed are limited and more capacity consequently is required to perform the enhancement functions.

In 1980, SRI International and COMSIS Corporation analyzed various design alternatives for the ARTS II enhancements. The technical advantages and disadvantages of each approach, relative life-cycle costs, and implementation strategies were considered.[*] On the basis of that study, SRI and COMSIS recommended that the existing LSI-2/20 be replaced with the larger, faster LSI-2/40. With a simple chassis change, the LSI-2/40 could be installed in the same cabinet space as the LSI-2/20. Because this computer is upgrade-compatible with the LSI-2/20, the current ARTS II programs are expected to run without any modification on the LSI-2/40. In addition, the existing I/O controllers and interfaces are directly compatible with the new computer. The LSI-2/40 provides up to 2.5 times the speed of the LSI-2/20 and has a memory expansion capability of 1 million bytes. As configured initially in ARTS IIA, it will have 512,000 bytes of memory--four times the maximum of the LSI-2/20.

The primary advantages of that recommendation are summarized as follows:

- Adoption of the LSI-2/40 is the lowest cost alternative.

- The alternative can be easily implemented.

- The equipment can be easily installed, and the sites can be easily converted; that is, there will be no physical changes, no space addition, and little effect on operations.

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[*]The results of that study are documented in Report FAA-RD-81-7, dated December 1980.

- Early and rapid deployment of hardware is possible, independent of computer program development.

- Qualified FAA and original systems vendor personnel are available to operate and maintain the system.

At the conclusion of that study, the FAA requested that SRI and COMSIS investigate several issues that had been raised regarding the LSI-2/40 hardware and software. Specifically, this study addressed:

- Validation and verification of the capabilities of a new power supply with an integrated backup battery providing for retention of the contents of the semiconductor memory of the LSI-2/40 during power line transients, including power failures of short duration.

- Validation and verification of code transportability.

- Validation and verification of the compatibility, performance, capacity, and reliability of the LSI-2/40.

Section II discusses the power supply required for a computer utilizing volatile semiconductor memory. Code compatibility between the existing and proposed computers is discussed in Section III. Section IV presents the results of experiments conducted to determine the speed of the LSI-2/40 in running actual ARTS II software. Estimated memory and CPU speed requirements of the various ARTS IIA enhancements are discussed in Section V; the air traffic environment forecast for 1990, the target time frame for the enhancements, is also discussed in that section. Section VI presents a summary and conclusions.

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II   POWER-FAIL RECOVERY

Current state-of-the-art computer systems rely on volatile semi-conductor memory. Thus, in replacing the LSI-2/20 with the LSI-2/40, the nonvolatile core memory currently used must be replaced with faster semiconductor memory. To retain data, the semiconductor memory requires continuous power. The limiting factor for ARTS II and ARTS IIA is that the hardware configuration does not include a high-speed mass storage device (such as a disk) that would provide a means to conserve vital data for a warm-restart/reload after a short-duration power outage or fluctuation. A power supply, memory unit, or other unit that includes an auxiliary battery power source thus must be incorporated into ARTS IIA. The battery would supply the voltage necessary to retain the contents of the memory during a power outage of from 2 to 30 minutes, power transient, or power fluctuation until the automatic or manual restart of the computer program is accomplished.

The following four alternative backup devices were deemed suitable for consideration during this study:

- On-board battery

- External battery

- Replacement power supply (battery backed)

- Uninterruptible AC power source (UPS).

The first three devices could be engineered and/or provided by Computer Automation as part of the LSI-2/40 hardware. UPS devices are standard and can be provided by a vendor specializing in this type of product; thus, no special engineering or modification would be required.

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With all these alternatives except the UPS, the computer processor chassis power supply would sense any power disruption and route an interrupt to the processor. This interrupt would freeze the processing and suspend execution of instructions in the CPU. At the end of the power disruption, the power supply would trigger another interrupt to the processor, initiating the execution of a program restart sequence using the computer memory (both data and program), which will have remained intact during the interruption of processing.

This sequence is essentially the same as that designed for the current ARTS II system. Because the current system merely maintains data related to target associations and flight plans, the sequence for program restart after a power outage does not depend on timing or on the duration of the interruption. In ARTS IIA, however, the operation of the safety functions and related processing depend on system timing, so that more than the simple retention of data must be considered in designing the methodology for program restart after a power interruption.

To identify the system that would provide the best backup, the project team assessed each of the four power-failure recovery alternatives, as described below.

On-Board Battery

The on-board battery was the most obvious choice for consideration because it is already among the memory products Computer Automation offers for the LSI-2/20 and LSI-2/40. Backup power is provided by on-board Ni-Cad batteries, which are maintained in a charged state by an integral charger circuit. This battery power is designed to maintain memory contents for up to 2 minutes during power interruptions.

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The 53819 memory board is available in 32KB, 64KB, and 128KB capacities. The preferable memory capacity specified for ARTS IIA, however, is 512KB. Two 53828 memory boards with 256KB capacity each thus were specified in the ARTS IIA configuration. The 53828 memory board cannot accommodate the on-board battery supply because of space limitations on the circuit board. Computer Automation did indicate that the 53828 memory board could be redesigned to provide a battery arrangement similar to that on the 53819 memory board.

The test plan for this study called for a demonstration at the Burroughs development facility in Denver, Colorado, of the 53819 memory board and LSI-2/40 CPU with MMU running ARTS II programs. This was intended to demonstrate the effectiveness of the on-board battery in providing protection from power failures for ARTS II. This approach would be applicable to any memory configuration available from Computer Automation.

The demonstration was not successful because of problems with the computer/device interface in the APC using the LSI-2/40 computer and chassis. These problems were attributed to electronic noise at the interface, which induced faults in the normal operation of the CPU and attached devices and caused the system to fail. As the study team later learned, the identical problem was encountered during the integration of the original ARTS II system hardware and was corrected through engineering analysis and design modification. Because of these problems, the tests for code compatibility and performance, which were run as part of this study and are described in Section III, were performed using the 53828 memory configuration.

The necessity for a hardware modification should not be considered as unusual or as evidence that the computer hardware is unsuitable; however, it precludes the use of the 53819 memory configuration until the bus terminations in the device interface are balanced to reduce

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electronic noise. The outcome of this test also indicates that the
system configuration must be validated at the APC level at an early
stage of the hardware quality assurance effort, because engineering
analyis and modification may delay development or testing of other
hardware or software components. Should deferring the decision about
the precise specifications of the computer hardware configuration be
necessary, adequate time must be allocated for testing and validation
of the device interface terminations.

External Battery

At the beginning of this study, Computer Automation representa-
tives had indicated that the 53828 memory boards might be redesigned
to incorporate an on-board battery capability similar to that of the
53819. In both of these memory boards, 16K-bit MOS chips are used.
This type of circuit requires DC voltages of +5V, +12V, and -12V and a
fully populated chassis to provide the overall capacities required by
the ARTS IIA system. Memory circuits based on the latest technology
are packaged in 64K-bit capacities and require only +5 DCV power.

This latest technology is the focus in Computer Automation's
current memory product design plans; consequently, in the redesign of
the 53828 memory board to provide backup battery protection, use of
the original type of memory circuit is unlikely. With the use of the
denser memory circuit capacities, the inherent problems in designing
auxiliary battery power circuitry are reduced (because of the require-
ment for only one voltage). In addition, the memory capacities on a
single board are increased by a factor of 4.

The availability of these new products by the fourth quarter of
1982 seems possible. Computer Automation most likely would include in
any such memory package, at least as an option, the provision for
attachment of an external battery power source, instead of one on the
memory board itself. Thus, to satisfy the ARTS IIA requirement for

memory backup, a small battery, a power supply, and charging electronics would need to be mounted within the APC cabinet. Only one such external system would be necessary, providing power to all memory boards. Should such a backup system be developed, the ARTS IIA hardware configuration specifications could be modified to substitute the new product for the 53828 memory.

For several of their models, other computer manufacturers do offer a feature external to the basic computer architecture to provide battery power for retaining data in memory during power outages. Appendix A presents brief descriptions of such options provided for minicomputers by IBM and Hewlett-Packard. These features are widely installed by both of these manufacturers, demonstrating the feasibility of such an approach for the protection of data in semiconductor memory. The list prices quoted for the features shown are between $650 and $2,200.

Battery-Backed Power Supply

During the early part of this study, one suggestion was that the system providing the ARTS II computer with DC power could be replaced with an off-the-shelf system that would automatically switch over to a battery power source to provide DC power during a short-duration power interruption. This battery-supplied power would be provided only to refresh the semiconductor memory and would not sustain continued processor operation. Computer Automation originally suggested this approach as a possible alternative to redesigning the memory products to provide on-board or external battery attachments. Rather than using an existing design, another possibility would be to commission a custom modification of another vendor's existing device that would provide the required capabilities. No vendor was found that offered such a device, however, so the custom modification approach was abandoned in favor of a redesign or retrofit of the Computer Automation memory products.

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Uninterruptible AC Power Source

The project team conducted a survey of several UPS vendors to determine the ability of the devices to provide protection for data in systems with semiconductor memory. The UPS units currently available are targeted to mini- and micro-computer systems and are no longer bulky and expensive devices that provide only higher capacity power requirements. Several vendors were identified as having a product that qualified, relative to specifications and cost, for serious consideration for use with ARTS IIA.

Appendix B presents information on the UPS supplied by Deltec Division of Gould, Inc., that is considered to be adequate to provide power for the processor of the ARTS IIA system. It consists of an AC power rectifier, inverter, battery reservoir, battery charger controls, transfer switch, RFI/EMI filter, and status indicators. The battery reservoir is a built-in gel-cell package with a 5-year maintenance-free life. The Static Transfer Switch is capable of a maximum 4-millisecond sense-and-switch time and make-before-break operation. The quoted price of this device with a 700-VA capacity is $3,500.

Figure 1 presents the configuration of an ARTS IIA system with a UPS. Such a configuration would supply power to the computer processor chassis, which consists of the central processor, memory and MMU, and I/O interfaces to the displays and DDAS. During a power interruption, the displays (RADS and BANS), DDAS, and presumably the radar and communications equipment would suffer a normal failure and ATC operations would be disrupted. The computer system powered by the UPS would continue to operate and would consider this condition as an apparent failure of the peripheral devices. It would continue to maintain (and age) target data until the quality of the data in the target store were degraded to the extent that a system cold-start were required. In either case, the capacity of the UPS to provide power would t. adequate, in the range of 5 to 10 minutes.

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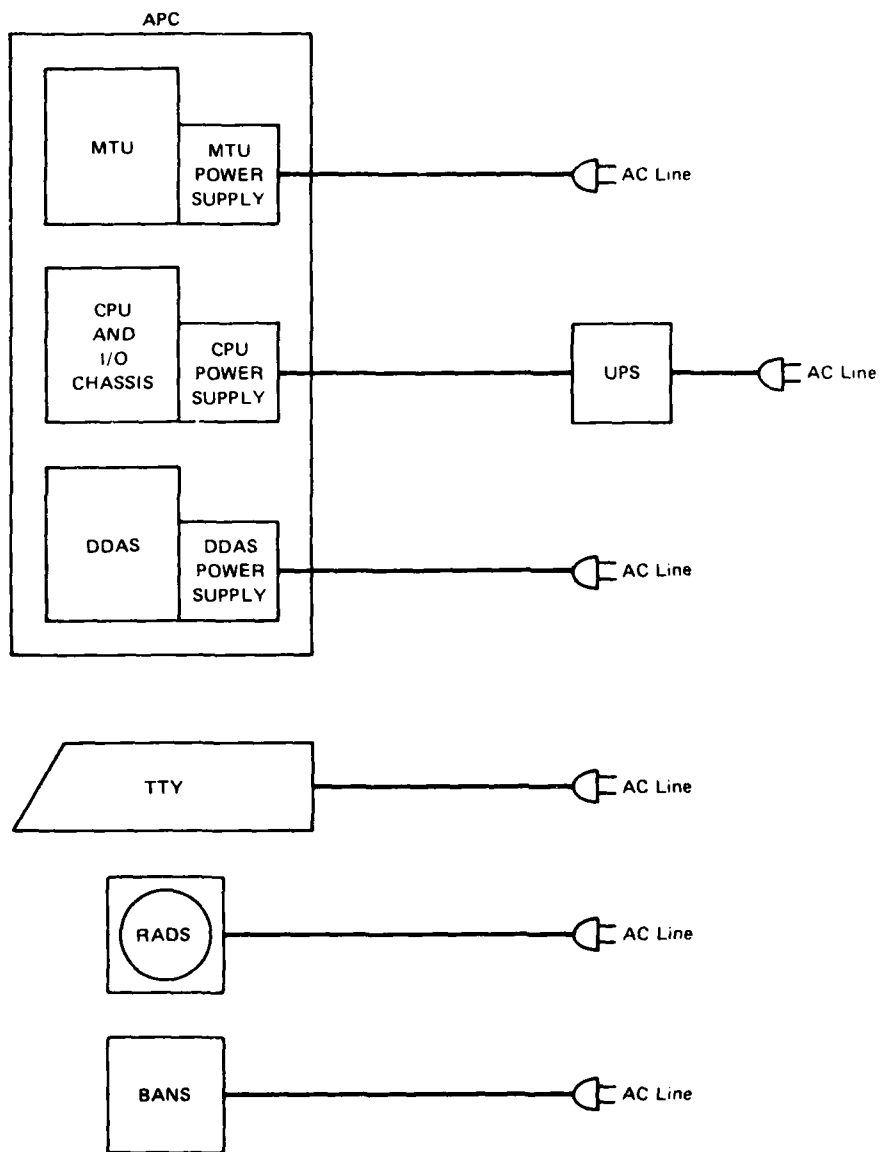
FIGURE 1   ARTS IIA CONFIGURATION WITH UPS

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The location of the UPS unit is not restricted to the APC cabinet or the immediate vicinity. It could be in any location convenient to AC line power, and a separate AC branch circuit could be wired to distribute the UPS output to the ARTS IIA computer.

The use of a UPS unit with ARTS IIA could provide additional operational benefits other than protection against memory data loss. Such a system would not only be protected during periods of power outage or fluctuation, but would also be protected from disruptions related to chronically poor power quality, which plague certain service areas and affect computer operation--even when other system devices such as radar and displays are not affected or recover more quickly than the computer system.

Recommended Alternative

Use of a UPS unit is the only alternative for memory protection that also provides an easy approach for a totally automatic (hands-off) restart of ARTS IIA operation once a power disruption ends. Because the computer processes continue, the data continue to be aged (track positions coasted, firmness levels reduced), and the clocks and timers used by the system continue to maintain correct values. The other methods of memory protection either do not offer a totally automatic restart capability or require additional hardware features for automatic restart, such as a battery-maintained time-of-day clock that the computer can read during a restart to restore the system time and determine the duration of the interruption. Nevertheless, any power-failure recovery methodology will affect the software systems design, and these all depend on the selected configuration of the hardware.

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III CODE COMPATIBILITY

The LSI-2/40 computer to be used for ARTS IIA will be installed
at the operational sites before the enhanced software has been
developed and tested. This independent installation of hardware and
software will result in minimal disruption to operations and in a
logical method of detecting and separating potential hardware and
software faults. To support this deployment plan, an objective of
this study was to determine the compatibility of the existing ARTS II
software with the LSI-2/40 computer.

This task was performed for the two types of ARTS II systems:
those requiring 32K words of memory and those requiring 40K words of
memory. The important difference between these systems is that the
40K systems are implemented with a memory banking scheme that must be
simulated with the MMU of the LSI-2/40. This situation does not arise
with the existing 32K systems because all memory required is within
the primary addressing range of the computer (15 bits).

32K Systems

Preliminary Test

Because all instructions, buffers, and the data base fit within
the primary address space of the LSI-2/40, no problem was expected in
running an existing site tape on that computer. To confirm this, we
used a system tape from FAATC configured for the ARTS II site at
Colorado Springs, Colorado. This tape was loaded onto the Burroughs
ARTS II development system in Denver, Colorado; neither the tape nor
the loader was modified. We used the Burroughs ARTS II static target
generater and the existing RADS to observe that the system operated

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and was stable. In addition, we performed a short checkout to verify that the basic ARTS II functions operated according to specification before we executed the ARTS baseline test.

Baseline Test

To verify correct operation of the 32K ARTS IIA program on the LSI-2/40 computer, we performed sections of the ARTS II Baseline Test Plan* for the A2.02 version. That test plan provides an on-site method to certify the proper functioning of the operational ARTS II computer program. The baseline test plan consists of the following four major categories of tests:

- Master control program

- Keyboard input program and keyboard test program

- IFDS processing

- General-purpose programs.

We performed the tests in the first two major categories in their entirety. Interfacility data processing could not be tested because the ARTS II development system was not interfaced to an ARTCC or an ARTCC simulator. The only test developed for general-purpose programs is that for the system performance summary, and it was not performed.

Master Control Program--To verify the master control program, 27 tests are conducted to ensure that the site-variable system parameters are adapted correctly for the site, and 3 tests are performed to ensure that teletype messages are being transmitted correctly. Of these 30 tests, 29 were performed as specified in the baseline test

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*The documentation of this plan was obtained from the NAS document facility at Atlantic City. The document bears no other identifying numbers or titles.

documentation; the results indicated correct operation. *The one test in* this category that was not performed involved the verification of interfacility error message printout; this test was not required because of the absence of interfacility interfacing.

Keyboard Input Program and Keyboard Test Program--The keyboard input and keyboard test programs comprise 1 test of the keyboard out and test pattern function, 21 tests of flight plan operations, and 12 tests of display control and systems configuration. These 34 tests were performed in accordance with the baseline test plan documentation, and the results indicated correct operation.

No deviations from correct operation occurred in any of the tests that were performed on the ARTS II software with the LSI-2/40 computer. These test results indicate that 32K ARTS II systems without inter- facility processing will run correctly on the LSI-2/40 at any operational site. The consistent excellence of these results gives us some assurance that 32K systems with interfacility processing will *also operate as* specified; appropriate certification tests have not been performed yet, however.

40K Systems

Modification of the System Tape

The 40K ARTS II system tape must be modified to operate properly on the LSI-2/40 because that computer has an MMU as opposed to the memory banking scheme of the LSI-2/20.

The primary function of the MMU is to translate the 16-bit logical address supplied by the processor into the 22-bit physical address required by the 8-megabyte memory subsystem. To accomplish this address translation, the MMU is configured around a page-oriented translation table. This translation table, which consists of a 1K-word RAM array,

is internally divided into 16 directories or maps. Each directory (map) provides 32 words (pointers), with each word acting as the translation medium for a 1K word memory block referred to as a page. Structuring the translation table in this manner provides each of the 16 directories with a full 32K words of memory address capability. Therefore, because each directory word performs address translation on a 1K word block of logical addresses, a processor-generated reference to a page of logical address locations may be mapped to any 1K block of physical memory. Furthermore, because the MMU is designed to output a 22-bit translated address in response to each 16-bit logical address, the 1K page being referenced may be located anywhere within the 8-megabyte memory system.[*]

The application of this system to ARTS II requires that two users (maps or directories) be established. Directory 0 addresses the first contiguous 32K of memory. In Directory 1, the first 24K of space is in common with that of Directory 0 and the last 8K as the 33rd through 40th K in memory.

Implementing this in code requires modification of four sections of ARTS II code. Three modifications are of existing code, and the fourth is the addition of a block of code for MMU translation table initialization. Exhibits 1 through 4 present these four sections of code. Together, they handle initialization of the system as well as power-fail and power-restart functions. The modifications of the first three sections of code were handled by directly modifying addresses in the ARTS II operational code. The large block of code (Exhibit 4) was implemented with the assembler. A new system tape was then produced for testing.

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[*]LSI-2 Series Memory Management Unit Reference Manual (53794-81); Computer Automation, Irvine, California.

Exhibit 1

PATCH IN SYSGO FOR SYSTEM INITIALIZATION

<u>ORIGINAL</u>

08BD	LXP	0
	LDA	F101

<u>MODIFIED</u>

JMP	SYSGOP

(Original code is now contained in patch.)

Exhibit 2

PATCH IN POWER-FAIL CODE

0167	INA	OE
	STA	BNKWD

Exhibit 3

PATCH IN POWER RESTART CODE

01B8	JST	RESTAR

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Exhibit 4

MMU INITIALIZATION ROUTINE
(Placed in Unused Memory)

```
*     FIX UP TRANSLATION TABLE IN MMU FOR 40K ARTS.
*     ENABLES TABLE ACCESS, SETS UP USER 0 AS FIRST
*     32K AND USER 1 WITH 24K COMMON WITH FIRST
*     24K OF USER 0, AND LAST 8K AS 33RD THROUGH
*     40TH K IN MEMORY.


DA        EQU       1             DEVICE ADDRESS OF MMU
          ORG       :5800         FREE SPACE IN 40K ARTS 2
PATCH     ENT                     SUBROUTINE ENTRY
          NOP                     SOME BLANK WORDS FOR PATCHES
          NOP
          NOP
          NOP
          NOP
          NOP
          NOP
          LAP       1             GET A ONE TO...
          OTA       DA,5             ENABLE TABLE ACCESS
          LDA       =:3000        WHAT GOES IN FIRST TABLE ENTRY
          STA       VALUE         STORE FOR LATER
          LDA       =:7C00        GET ADDR OF TRANS TABLE
          STA       ADDR          STORE FOR LATER
          AAI       :40           INC TO POINT TO USER 1
          STA       ADDR2         STORE FOR LATER ALSO
          LAM       :20           GET COUNTER:  # OF WORDS TO SET
          STA       COUNT         STORE... 32 STEPS
LOOP1     EQU       $             SETTING UP BOTH USERS LOOP
          LDA       VALUE         GET TABLE VALUE
          STA       *ADDR         STORE IN USER 0
          STA       *ADDR2            AND USER 1
          IMS       VALUE         INCREMENT THE TABLE VALUE
          IMS       ADDR          INC. PTR TO USER 0 SPACE
          IMS       ADDR2         INC. PTR TO USER 1 SPACE (ENTRIES)
          IMS       COUNT         INC. AND CHECK THE COUNTER
          JMP       LOOP1         LOOP BACK IF NOT YET ZERO
*
*     NOW FIX UP THE LAST 8 K OF USER 1
*
          LDA       =:7C58        GET PTR TO ENTRIES, LAST 8 K
          STA       ADDR          STORE
          LDA       =:3020        GET VALUE TO GO IN FIRST ONE
          STA       VALUE         STORE
          LAM       8             GET COUNTER VALUE
          STA       COUNT         STORE
LOOP2     EQU       $             FIX UP USER 1 LOOP
          LDA       VALUE         GET THE VALUE
```

Exhibit 4 (continued)

```
          STA        *ADDR         STORE INTO TABLE ENTRY
          IMS        VALUE         INCREMENT THE VALUE
          IMS        ADDR          INC. THE PTR TO ENTRY
          IMS        COUNT         INCREMENT AND CHECK THE COUNTER
          JUMP       LOOP2         RETURN IF NOT DONE YET
*
*    CLEANUP LOGIC.  ENABLE TRANSLATION, INCREMENT THE
*    RETURN ADDRESS, AND RETURN
*

          LAP        2             GET CONSTANT TO ENABLE TRANSLATION
          OTA        DA,5          OUTPUT THE STATUS
          IMS        PATCH         INC. RETURN ADDR
          RTN        PATCH         RETURN TO CALLER
*
*    BEGIN DATA
*
COUNT     RES        1,0
VALUE     RES        1,0
ADDR      RES        1,0           PTR INTO TRANS TABLE, USER 0
ADDR2     RES        1,0           PTR IN TRANS TBL,   USER 1
          LPOOL


*
* PATCH TO USE WHEN RESTARTING THE ARTS II AFTER A
* POWER FAILURE.  RELOADS THE USER AND DMA REGISTERS
* WITH WHAT THEY HAD AT THE TIME OF THE FAILURE,
* CALLS THE PATCH TO SET UP THE TRANSLATION TABLE,
* AND RETURNS TO THE POWER FAIL CODE TO DO THE REST.
*
RESTAR    ENT                      SUBROUTINE ENTRY
          OTA        DA,4          RESET THE MMU
          LDA        *BNKWRD       GET THE FORMER USER REGISTER CONT
          LRA        4             SHIFT DMA # TO BOTTOM
          OTA        DA,7          OUTPUT TO MMU
          LDA        *BNKWRD       GET THE WORD AGAIN
          OTA        DA,6          SET THE USER REGISTER
          JST        *$+1          GOT TO THE SETUP ROUTINE
          DATA       PATCH         ADDR OF THE TRANSLATION TABLE SET
          IMS        RESTAR        INC. RETURN ADDR
          RTN        RESTAR        RETURN
BNKWRD    DATA       :16C          ADDR OF BANKER WORD
*             IN POWER FAIL CODE
*
*    CODE TO DO WHEN PERFORMING SYSGO
SYSGOP    ENT                      SYGO PATCH
          OTA        DA,4          RESET THE MMU
          LAP        0
          OTA        DA,6          SET USER REGISTER
```

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Exhibit 4 (concluded)

```
            LAP        1               GET ONE TO...
            OTA        DA,7            SET DMA INDEX REG
            JST        *$+1            JUMP TO REINIT CODE
            DATA       PATCH           ADDR OF TABLE SETUP CODE
C400        LXP        0
B202        LDA        F101
            IMS        SYSGOP          INC. RETURN ADDR
            RTN        SYSGOP          RETURN
F101        DATA       :F101
            END
```

Baseline Test

To verify operation of the 40K ARTS system on the LSI-2/40, we performed a subset of the A2.02 baseline test plan rather than the entire test. In performing the baseline test for the 32K system, we realized that the majority of functions within each of the three main categories were similar and that performing all the tests was not necessary to reveal obvious operational insufficiencies. Consequently, we decided to perform 19 of the 30 tests of the master control program for the 40K system. Seven of the 34 tests of the keyboard input program and keyboard test program were also performed. The system responded to inputs as specified. The 40K system performed as well as the 32K system on operational tests; however, the power-fail restart capabilities were not examined because the memory in the test system did not contain a backup battery. Therefore, no conclusions can be made about the adequacy of the code in Exhibits 2 and 3. Other than that, we conclude that the 40K system with MMU will perform correctly with the code modifications in Exhibits 1 and 4.

Nonoperational Programs

In addition to the operational ARTS II program, several programs used at FAATC must be verified on the LSI-2/40: the assembler, various editors, and the loader. The project team performed this verification during two visits to the Burroughs development facility in Colorado by observing program development on a system in which the LSI-2/20 and LSI-2/40 could be used interchangeably. Because none of the nonoperational programs require more than 32K words of memory for operation, the existence of the MMU had no effect on these programs. We therefore are confident that all nonoperational programs will operate correctly on the LSI-2/40.

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IV COMPUTER SPEED

One of the basic questions in developing the ARTS IIA system is whether the speed of the LSI-2/40 computer in overall operation is sufficient to handle the additional work load imposed by the enhancements. One of the objectives of this project was to determine the overall ratio in speeds between the LSI-2/40 and the LSI-2/20 in executing the actual ARTS II code. The experiments conducted to determine this ratio also enabled us to determine excess CPU capacity, that is, the amount of CPU available for the ARTS IIA enhancements.

To perform these experiments, we used the ARTS II development system at Burroughs Corporation in Denver, Colorado. This system consisted of an APC, three RADS, and a BANS. In addition, a static target generator was available to produce both beacon and primary radar video signals as input. This development system was originally configured with the standard LSI-2/20 computer and 40K words of memory. An LSI-2/40 computer with 256K words of memory was available for replacement in the APC as required. Thus, we were able to run ARTS II code with both the current and proposed computers. Exchanging computers required approximately 0.5 hour.[*] The basic switching operation consisted of unsnapping the computer console front panel and unplugging the console cable for the computer mother board. The I/O cables were unplugged from the front and back of the computer: TTY,

_____

*The computer exchange was not representative of the operations that will take place at each site when the LSI-2/20 is replaced with the LSI-2/40. We did not, for example, replace the power supply. Further, to facilitate rapid exchanges, we did not mount the computers in the APC but merely connected them electrically.

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memory banker cable (40K system only), Burroughs' cables to the lower chassis. The power supply cable was disconnected from the computer. These operations were reversed for the new computer.

The static target generator in the Burroughs development system was that used in the development of the original ARTS II system. Exhibit 5 presents the switch settings used for all tests in this experiment. In addition, we used a universal counter to measure the speed of the computers in the manner described below and an oscilloscope to examine various pulses for detailed measurement.

Baseline Measurements

The basic method for measuring the speed of both the LSI-2/20 and LSI-2/40 computers in the ARTS II system was to replace one instruction in the master executive loop so as to produce a pulse at an output port. This nine-instruction loop is executed when the computer is not servicing any interrupts or executing any other routines as specified by the timer. Therefore, any time spent in this idle loop can be considered as available CPU time.

The idle loop is an actual software loop and was modified to produce a single output pulse each time it was executed. Thus, determining available CPU time is possible by counting output pulses in a specified interval. The interval used in this experiment was the scan period, as determined by a signal from the static target generator. This interval was approximately 3.87 seconds; a signal from the static target generator was used to open and close the counting gate in the universal counter to produce a reading over that interval. The oscilloscope was used to observe the output pulses during steady-state conditions as a check of the universal counter readings.

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Exhibit 5

STATIC TARGET GENERATOR SETUP

M3A:	AS REQ'D
MC:	AS REQ'D
SPI:	AS REQ'D
XBIT:	OFF
DELAY SELECTOR:	1
DELAYED ELEMENT:	OFF
TGTS/SWEEP:	$(12)_8 = 10$
TGT WIDTH:	$(13)_8 = 11$
PATTERN REPEAT:	$(100)_8$
TGTS/SCAN:	AS REQ'D
SPACING:	4 MI
BEACON:	ON
RING:	OFF
PATTERN SYNCH:	ON
TGTS/SWEEP AUTO LIMIT:	OFF
FIXED MAP INHIBIT:	OFF
SENSOR ALARM:	OFF
TRIGGER MODE:	UNSTAGGERED

Exhibit 6 shows the original idle loop, with the single instruction modification necessary to produce the output pulse. The IMS instruction was used to increment an idle loop counter; this could not be used in real time because the system would have to be shut down to check the contents. The SEL instruction with which it is replaced sends function code 3 to device 31, the buffer board. This function code is not used by the buffer board but is decoded nonetheless; a pulse is produced at the output of the function decoder.

We measured the idle loop execution speed by turning off the interrupt system and producing no targets from the static target generator. When the interrupt system was disabled, the RADS and BANS were not serviced; with no input targets, no routines were executed other than the idle loop itself. The LSI-2/40 executed the idle loop in 7.5 microseconds, equivalent to a pulse count of 514,300 in the 3.87-second interval. The 7.5-microsecond speed was also observed on the oscilloscope to the limits of its resolution. In addition, we checked this figure by attempting to determine the execution time of the nine instructions in the idle loop. The theoretical time for execution of the loop was 8 microseconds. This 6.25% difference (the actual execution was faster than the published time) can be attributed to experimental measurement error and to the fact that the memory in the LSI-2/40 was different from that specified in the computer manual.

Mounted on the MMU board was a three-position toggle switch, the positions being cache on, cache off, and cache controlled by software. We used the cache on and cache off positions initially to test various speed assumptions; thereafter, the cache was on in all experiments. With the cache off, the LSI-2/40 executed the idle loop in approximately 12 microseconds. This rather large speed differential from the 7.5 microseconds with the cache on testifies to the extreme power of cache.

Exhibit 6

CHANGE IN IDLE LOOP TO ALLOW REAL-TIME MEASUREMENT

```
        INTQ    EQU     $
                SIN     4
                LDX     FIFOG:
                LDA     @CHAIN
                JXZ     XQT

        *        .
        *        .      FIFO QUEUE PROCESSING INSTRUCTIONS
        *        .

        XQT     EQU     $
                LDX     READY:
                JXN     $+4
                IMS     IDLE        Replace by      SEL  31,3
                NOP
                JMP     INTQ
```

The LSI-2/20 produced a count of 242,100 in the 3.87-second scan interval, equivalent to an idle loop time of 16 microseconds. This compares with the computed value of 15.5 microseconds for execution time. Thus, with the cache on, the LSI-2/40 is 1.88 times faster than the LSI-2/20 in executing the idle loop. This loop is not composed of a representative set of instructions, but comparing these execution speeds with the speed ratios that resulted from experiments described below is instructive. Note also that the counter readings did very when a single experiment was repeated--even the measurement of the idle loop. (For example, the LSI-2/40 idle loop count when measured with cache on varied between 514,100 and 514,350). This difference was always less than 0.05% and was assumed to be negligible in all measurements.

Determination of the Speed of the LSI-2/40

The speed of the LSI-2/40 was measured with variation in the following items:

- Total number of targets

- Number of displays

- Number of associated targets.

In addition, measurements were made when the system was configured for a given number of output devices but with fewer of them actually turned on. This offered a useful representation of the amount of CPU time required to build and maintain a single buffer area, but our efforts were based on the assumption that the system would be configured for the number of devices actually used.

For an experiment involving a specific number of displays, the measurement procedure was to increase the number of targets from 0 to 200 in intervals of 50 and measure the output pulse after each change; then the process was repeated while the number of associated targets

for each group of total targets was increased. The number of associated targets was either 0, 24, 45 or 48, or 72. All associated targets were divided among all the displays that were turned on at the time. Thus, the maximum load studied was 200 targets, of which 72 were associated, divided among 3 RADS and 1 BANS.

Results for the 32K Systems

These experiments also indicated the percentage of CPU available. Figures 2 through 5 present the results obtained for 0, 24, 45 or 48, and 72 associated targets for the LSI-2/40 with cache on, running the 32K ARTS II system configured for Colorado Springs, Colorado. In each case, the percentage of CPU utilization was derived by dividing the counter reading by the idle loop count.

These results are summarized and projected in Figure 6. The solid lines indicate actual experimental results covering 1 through 4 displays; the dashed lines are straight-line projections of the percentage of CPU available covering 5 through the maximum of 11 displays. Note that no reference is made to the number of associated targets. The expectatation would be that for more associated targets, less CPU would be available because of the increase in DMA activity required to display the tags for each associated aircraft. In reality, this effect is relatively minor, as indicated by comparing Figures 2 through 5. Figure 7 indicates the percentage of utilization required per additional display as a function of total targets and number of associated targets. Note that for 150 targets and fewer, the difference in utilization per display between 0 and 72 associated targets is less than 0.3%. The straight-line projections in Figure 6 were derived from the straight line produced by fitting the points in Figure 7. Thus, the maximum error due to associated targets would

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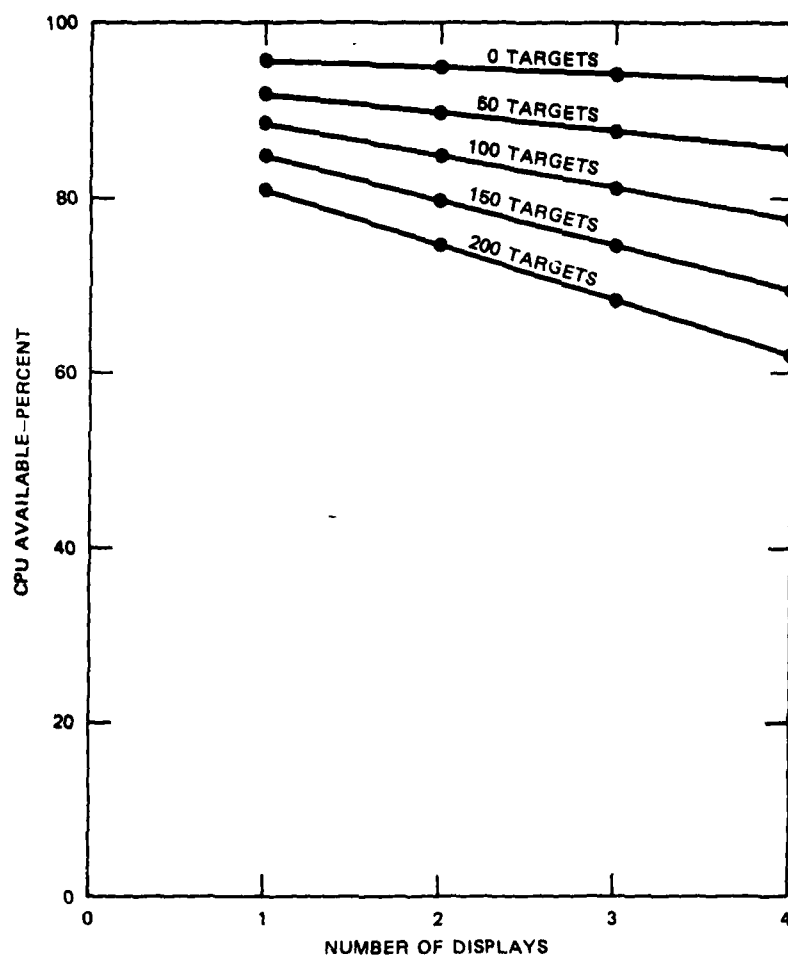
FIGURE 2   LSI-2/40 AVAILABLE WITH 0 ASSOCIATED TARGETS

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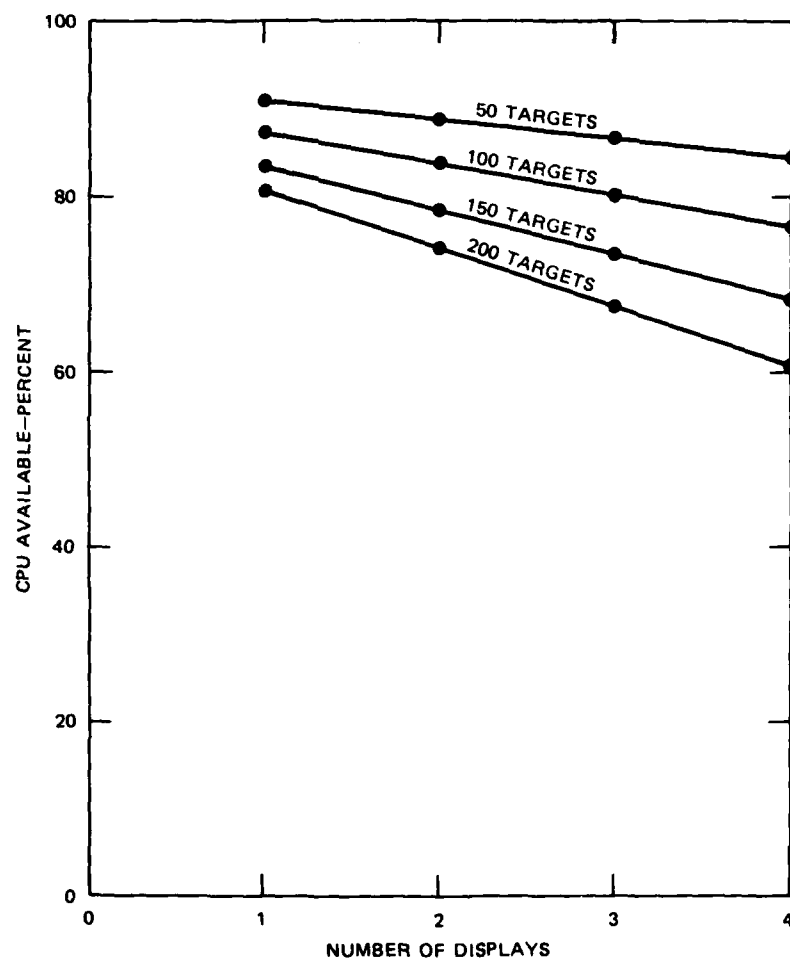
FIGURE 3   LSI-2/40 AVAILABLE WITH 24 ASSOCIATED TARGETS

29
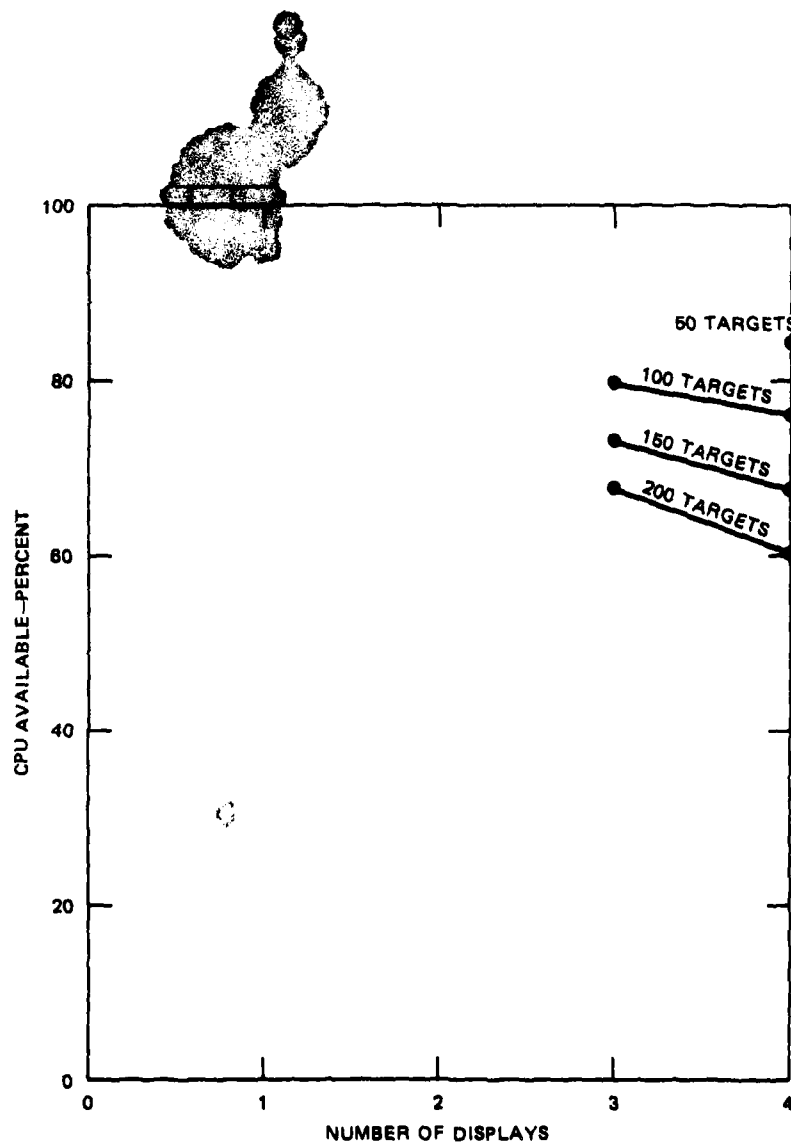
FIGURE 4   LSI-2/40 AVAILABLE WITH 45 TO 48 ASSOCIATED TARGETS

30
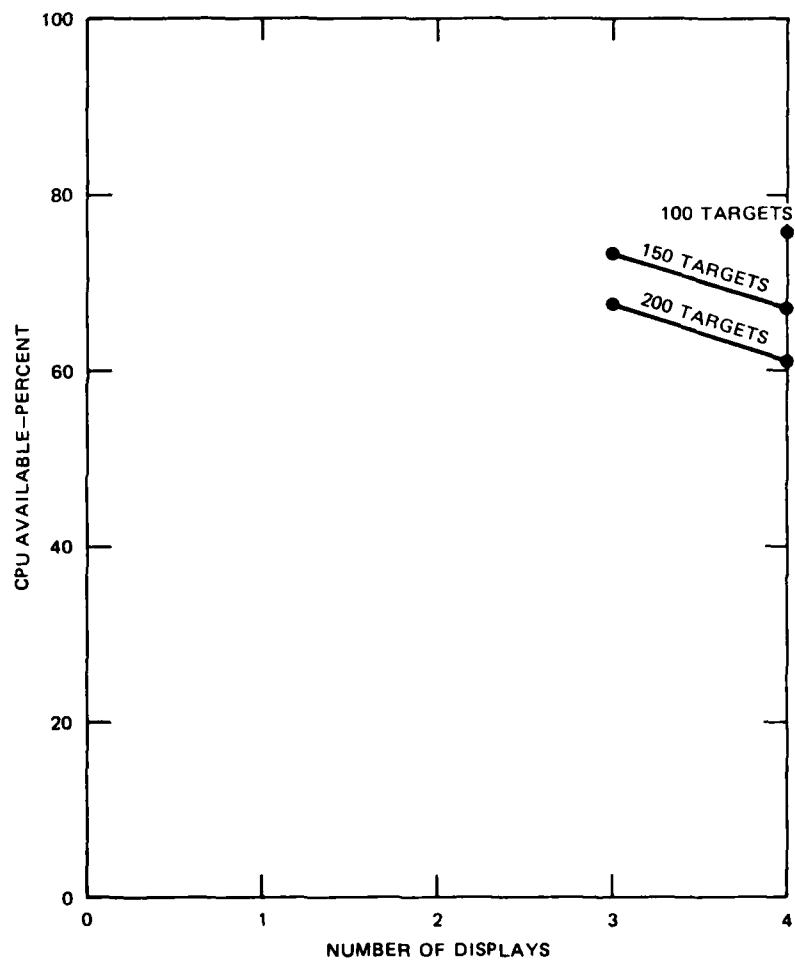
FIGURE 5   LSI-2/40 AVAILABLE WITH 72 ASSOCIATED TARGETS

31
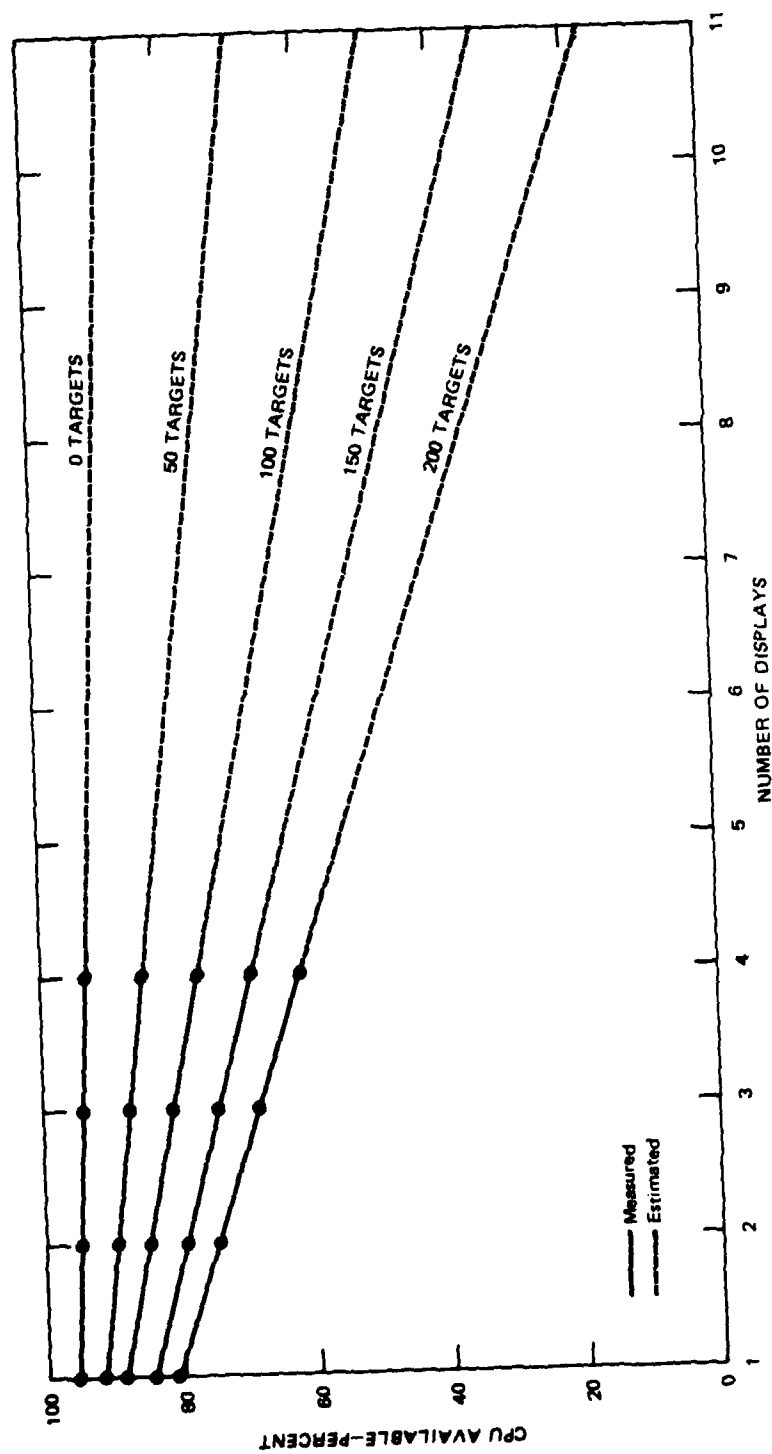
FIGURE 6   LSI-2/40 PROJECTED AVAILABILITY

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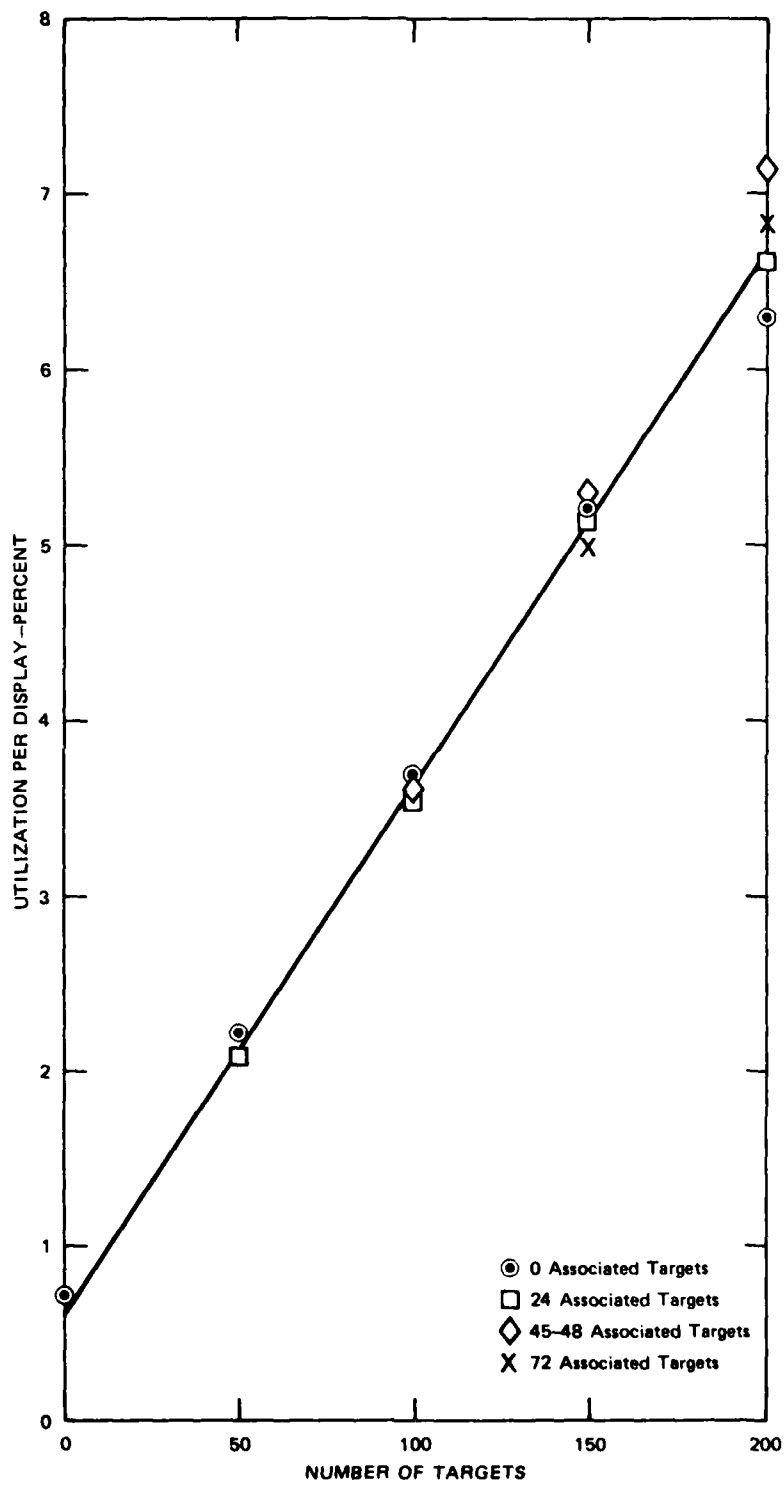
FIGURE 7   LSI-2/40 UTILIZATION PER DISPLAY

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occur at 200 total targets and 11 displays and could be represented on Figure 6 by a band around the line for 200 targets of plus or minus 6.6% for 11 displays.*

We performed detailed experiments to confirm the apparent insensitivity to the number of associated targets. Figure 8 shows the idle loop count and percentage of CPU available for 50 targets on a single display. As the number of associated targets increases from 0 to 30 (60% of total), the idle loop count and percentage of CPU available follow a smooth curve. With more than 30 associated targets, no further reduction in CPU availability is evident, even though more DMA time is required to output the two-line target tag. This confirms our expectation that efficiencies in processing compensate for additional I/O servicing with relatively high percentages of associated targets.

Results for the 40K System

A 40K system was loaded and tested for a relatively limited number of data points. The results generally indicated that the execution time of the 40K system will be as fast as that of the 32K system with MMU and cache on. Measured differences were less than 1% and did not indicate any specific trend.

Comparison of the Speeds of the LSI-2/40 and LSI-2/20

Figure 9 presents the results of measuring the percentage of CPU available on the LSI-2/20. This illustration cannot be compared with Figure 6 because each represents the CPU available on a specific

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*Figure 7 was derived from averages of measurements taken in the field. At 200 targets, the maximum difference of utilization per display is approximately 0.6% (between 0 and 72 associated targets). This difference at a maximum of 11 displays yields a possible variation of ± 6.6%.
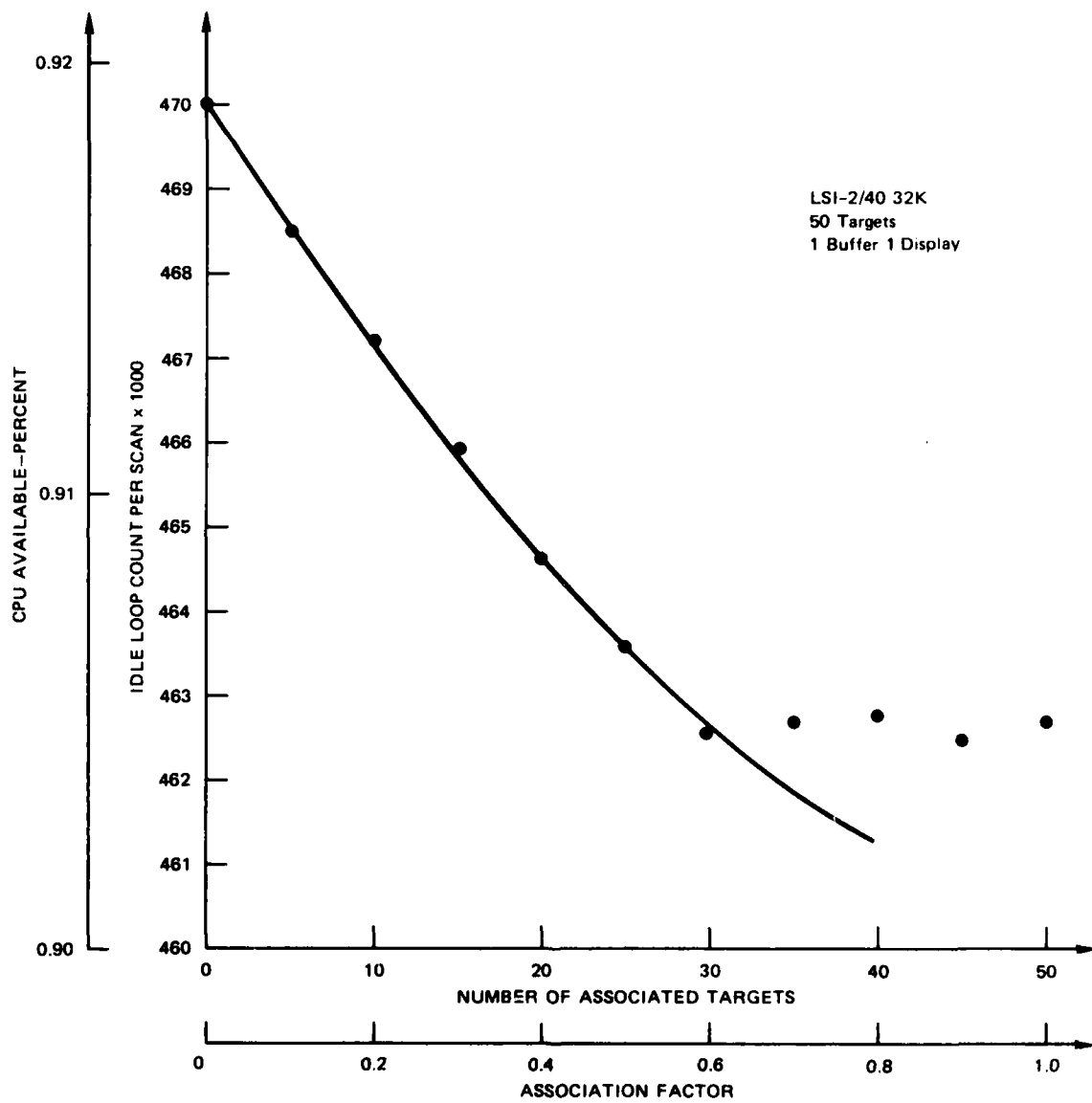
FIGURE 8   LSI-2/40 AVAILABLE

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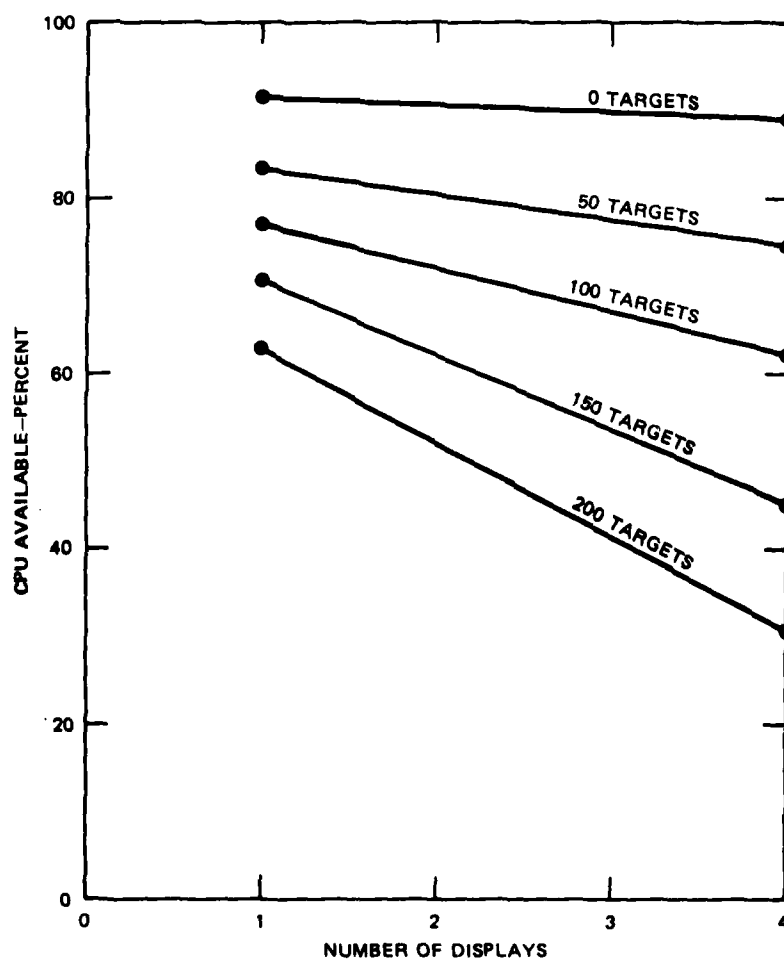
FIGURE 9   LSI-2/20 AVAILABLE

computer. Because of the difference in speeds between the computers,
1% of the LSI-2/40 represents approximately 1.88 more time than 1% on
the LSI-2/20.

The LSI-2/40 was, however, approximately 1.8 times faster than
the LSI-2/20 for a small number of targets and ranged up to 1.9 times
faster for 200 targets (for a single display). This trend is
reasonable: As the number of targets increases and the amount of
processing required increases, the increased speed of the LSI-2/40
gives it a clear advantage. As the number of displays increases,
however, the speed differential decreases because the DMA rate for
both computers is the same.

V ENHANCEMENT REQUIREMENTS

The LSI-2/20 computer approaches saturation under high aircraft loads when configured for a large number of displays. In addition, the program, data areas, and buffers require up to 40K words of the maximum 64K.* The addition of enhancement functions thus requires the substitution of a computer with additional processing speed and the capability to store and run larger programs.

One of the objectives of this project was to estimate the memory and CPU speed required to implement the ARTS IIA enhancements on the LSI-2/40 computer. MSAW, CA, and tracking (required for MSAW and CA) constitute the safety enhancements; TTG is for training and functional testing of operational programs and thus is not a safety-related function. TTG is used only when time is available on the system, so it was not considered in the determination of CPU speed requirements.

In this section, estimates and comparisons are presented for algorithm execution speed and computer utilization for a single aircraft as well as for 64 aircraft tracks. This is not to imply the requirement for 64-track capacity. It is merely useful because IOP measurements are available for 64 tracks, which provide an estimate of actual utilization for a reasonable processing load.

Memory Required

Table 1 indicates the amount of memory currently used in implementing the safety enhancements on the ARTS III IOP-B, including program and data. Because this Univac machine contains 30-bit

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*Even the maximum of 64K words, achieved with memory banking, cannot be used for program expansion; it is limited to buffer space for additional displays.

Table 1

MEMORY REQUIREMENTS FOR SAFETY ENHANCEMENTS

Enhancement	IOP (30-bit words)	LSI-2/40 (16-bit words)
Tracking		
Program	1,850	3,700
Tables and data*	1,498	2,996
CA		
Program	4,920	9,840
Tables and Data+	1,481	2,962
MSAW		
Program**	3,200	6,400
Total	12,949	25,898

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*Assuming 64 tracks.

+Assuming 64 tracks, 11 displays, 1 primary airport (Type I Area), 4 approach areas (Type II), and 8 legs (Type III).

**MSAW tables and data included in tracking.

registers and memory, these figures must be converted into memory requirements for the 16-bit-word LSI-2 series computers. To first order, a ratio of 30 to 16 can be used on the assumption that both program and data base memory will be used as efficiently as possible in both machines. In the worst case, a ratio of 2 to 1 can be used, assuming that each 30-bit word will require a double word on the LSI-2. Even so, the total memory requirement for the enhancements should not be more than 30K words, allowing a comfortable margin in the initial ARTS IIA configuration of 256K words (512K bytes).

CPU Speed Required

An analysis of CPU speed required to perform the enhancements is necessary to determine whether the computer can perform those functions in addition to existing tasks under given loads of aircraft and displays. Specifically, the analysis must determine the combination of number of displays, instantaneous airborne count (beacon equipped), and associated aircraft (discrete beacon code and Mode C equipped, for which the enhancement services are provided) at which computer saturation occurs.

The software for MSAW, CA, and tracking has not yet been designed or coded for the LSI-2/40, which leads to difficulty in making saturation estimates. Software designs and their corresponding implementation strategies can vary greatly relative to execution time and yet still perform the same function. Moreover, even though a software design exists for the safety enhancements on the IOP, extrapolating the execution times for those functions to the LSI-2/40 is complicated by the architectural differences between the two computers.

The primary differences between the IOP and LSI-2/40 architectures become apparent when their respective instruction sets are examined: The IOP has seven index registers, whereas the LSI-2/40 has one; the IOP has two 30-bit arithmetic registers, whereas the LSI-2/40 has one

16-bit register; and the LSI-2/40 supports indirect memory addressing, whereas the IOP has no support for indirect addressing but supports memory-extended addressing.

Assuming that these architectural differences can be overcome, any estimate of CPU speed will only be as accurate as the software design is appropriate for the IOP architecture and will not reflect any improvements in the software designed for the LSI-2/40. The ARTS III software designs probably are not the best designs for the LSI-2/40. Consequently, the project team assumed that any new software designed for the LSI-2/40 will utilize improved hardware facilities and thus will perform as well as or better than the ARTS III software operates on the IOP. This assumption enabled us to focus on the worst-case design and performance conditions. The approach described here for estimating CPU capacity requirements was designed to overcome these difficulties and to produce results accurate enough to be used constructively and confidently.

Estimation Technique

The ARTS III operational software was used to estimate the CPU capacity requirements for the ARTS IIA safety enhancement modules on the LSI-2/40 processor because it contains all the modules and because the source code and machine documentation are readily available. The ARTS IIA safety modules are expected to be functional copies of their proven and tested ARTS III analogs.

An execution time conversion technique was used, whereby we calculated the execution time of each equivalent IOP instruction on the LSI-2/40. These calculations were then used to estimate, with the aid

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of a computer program,[*] the CPU requirements to execute an IOP module on the LSI-2/40. The technique was applied to the MSAW module to generate a performance ratio for the two computers. This ratio was in turn used to estimate the execution time of the other safety enhancement modules on the LSI-2/40.

The MSAW module was selected as the primary conversion module because it is the least complex of the ARTS IIA modules. It has the fewest lines of code, facilitating entry of the code into a computer program as data. MSAW also has the attribute of handling only one track at a time (compared with CA, the execution time of which depends greatly on the position and movement of pairs of aircraft). Compared with the other modules, MSAW embodies the simplest execution logic; it has three main paths, one of which is executed for each track in the system.[+] In addition, the level of arithmetic computation in MSAW is lower than that in the CA or tracking modules, thus reducing some of the error inherent in this estimation technique due to the inability to incorporate the difference in word sizes for the IOP and LSI-2/40 into arithmetic calculations. The MSAW module was considered to contain a representative instruction mix, having 43% load/store memory reference instructions, 0.7% program control instructions, 29% arithmetic instructions, 9% implied load/store arithmetic, and 2% hardware-related instructions.

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[*]This WATFOR program uses IOP assembler language code as input and has data stored on the execution times of IOP instructions and on the execution times of equivalent LSI-2/40 instructions. The program was constructed as a simple calculator tool to permit quick computation of execution times for routines or multiple executions of blocks of code within routines.

[+]Primary airport approach monitor, general terrain monitor, and satellite approach monitor.

For the purpose of simulation, the general-purpose registers of the IOF were implemented as memory locations. No compensations were made for the smaller word size of the LSI-2/40 or for differences in the addressing modes of the two machines. For instructions having more than one time specification, the longest execution time was selected, except for main memory variations, for which the 500-nanosecond IOP core memory was assumed. In this conversion, we did not attempt to replace IOP instructions that had no equivalents in the instruction set for the LSI-2/40. These instructions usually pertained to control of specific hardware and processor features not available on the LSI-2/40. The percentage of these instructions contained within the MSAW module was analyzed and considered to be insignificant.

In the conversion, we used the execution times published by the vendor for each machine. For each instruction in the IOP instruction set, we identified the functional equivalent in the LSI-2/40 instruction set. The execution time for each instruction in the IOP set was then replaced by the execution time or the sum of the execution times for its equivalent in the LSI-2/40 instruction set. This effectively maps the functional execution timings from one instruction set to another and from one processor to another.

As an example, consider the load accumulator instruction (LA) for the IOP, which has a single-instruction functional equivalent (LDA) in the LSI-2/40 instruction set. A more complex conversion is required for an IOP instruction such as LSUM (load sum of register Q + Y OPERAND into accumulator), which has no direct equivalent instruction in the LSI-2/40 instruction set. In this instance, we replaced the single-instruction execution time for the IOP with the set of instructions for the LSI-2/40 that are functionally equivalent--that is, LDA QREG, ADD YREG. Other instructions in this no-equivalent category are LDIF, LLP, LSUM, RD, RDIF, RI, RA, RAN, RLP, ROR, RSUM, and RXOR.

The MSAW code and instruction execution times for the two machines were used to produce simulated execution time. This conversion method can be tested for its relative accuracy by comparing the results from sample time and previously published performance benchmarks on the ARTS III MSAW module. This check is not an absolute indicator because the site adaptation and the general terrain map denote the amount of work MSAW must actually perform, but it does flag any large miscalculations.

With this technique, any portion of the code can be extracted to analyze various logic paths. Common subroutines can be selected and extracted for simulated times. For MSAW, simulated times were obtained for the three major logic paths of execution (approach monitor, primary airport, and satellite airport) and all subroutines, including issuance of the MSAW warning.

The actual estimation process required first that the execution-controlling parameters (number of aircraft and their location relative to the primary airport) of the module be determined. These parameters were then varied to simulate all major control paths though the module including best-case as well as worst-case execution logic. The MSAW code portions that performed each of the simulated executions were then isolated in preparation for the simulated executions.

The second step was to actually quantify the execution time of those major paths. This was performed by accumulating each type of instruction within the path and totaling the converted execution time. Subsequently, the subroutines called were totaled, multiplied by their respective execution times, and included in the total execution time for that run. The resultant figure represented the estimated execution time of that path on the LSI-2/40 and therefore an estimation of the CPU requirements for a given set of execution parameters.

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In addition, a total block execution estimation was performed on the MSAW module. This total block estimation assumed no parameterized control execution and thus essentially estimated the CPU requirements to execute every instruction in the module. The resulting figure can be viewed as an absolute worst-case execution of the module and CPU capacity requirements.

The execution control parameters for the MSAW module were determined for a number of different execution paths. One of three major paths was executed for each aircraft depending on whether the aircraft was on the glide path of the primary airport, within the vicinity of the primary airport, or within the vicinity of a satellite airport. The worst-case execution for each of the major paths was one in which the aircraft did not pass the safe altitude criteria, thus generating a minimum safe altitude warning.

Determination of CPU Required for MSAW

Tables 2 through 4 present the results of the simulated MSAW executions, indicating the CPU requirements per aircraft and per 64 aircraft (as specified by the FAA) with and without generation of a minimum safe altitude warning. Note that the CPU requirements are strictly for the MSAW module itself. Table 5 summarizes these results. Acutal incorporation of the modules into the system requires additional processing by the tracker and other components. Table 6 shows the amount of IOP CPU required for these additional functions. The LSI-2/40 CPU requirements, also shown in Table 6, were derived by multiplying the IOP requirement by the average performance factors from Tables 2 through 4 (approximately 13% reductions).

The resultant ratios are indicators of the worst-case performance improvement of the LSI-2/40 over the IOP for MSAW and the other ARTS IIA safety enhancements. The conversion proved to be a relatively accurate measurement tool for the purpose of estimating CPU requirements.

Table 2

RESULTS OF THE SIMULATION OF THE MSAW
PRIMARY AIRPORT APPROACH MONITOR

	IOP (μs)	LSI-2/40 (μs)	Performance Improvement(%)
Time to execute full logic sequence	341.53	344.22	
Time to execute subroutines	732.66	591.05	
RUNXY	(219.94)	(179.90)	
CKVIOY	(2.96)	(2.60)	
TROBXY (4 calls)	(485.12)	(388.8)	
BACKPY	(24.64)	(19.75)	
Total without warning	1,074.19	935.27	
Time to produce warning	145.89	123.15	
Total with warning	1,220.08	1,058.42	
CPU utilization per aircraft without warning* (%)	0.028	0.024	12.9
CPU utilization per aircraft with warning (%)	0.032	0.027	13.3
CPU utilization for 64 aircraft without warning (%)	1.80	1.57	12.9
CPU utilization for 64 aircraft with warning (%)	2.05	1.78	13.3

*Assuming 3.87-second scan period.

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Table 3

RESULTS OF THE SIMULATION OF THE MSAW GENERAL TERRAIN MONITOR

	IOP (μs)	LSI-2/40 (μs)	Performance Improvement(%)
Time to execute full logic sequence	719.10	619.20	
Time to execute subroutines	1,097.69	936.87	
BINCH2 (14 calls)	(1,016.12)	(865.90)	
CMPUT2	(14.77)	(11.55)	
YCROS2 (2 calls)	(66.80)	(58.62)	
Total without warning	1,816.79	1,556.07	
Time to produce warning	145.89	123.15	
Total with warning	1,962.68	1,679.22	
CPU utilization per aircraft without warning (%)	0.048	0.041	14.4
CPU utilization per aircraft with warning (%)	0.051	0.044	14.4
CPU utilization for 64 aircraft without warning(%)	3.07	2.62	14.4
CPU utilization for 64 aircraft with warning (%)	3.26	2.82	14.4

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Table 4

RESULTS OF THE SIMULATION OF THE MSAW SATELLITE APPROACH MONITOR

	IOP (μs)	LSI-2/40 (μs)	Peformance Improvement(%)
Time to execute full logic sequence	361.64	357.78	
Time to execute subroutines	745.98	607.90	
RUNXY	(219.94)	(179.90)	
COMHY	(16.28)	(19.45)	
TROBXY (4 calls)	(485.12)	(388.80)	
BACKPY	(24.64)	(19.75)	
Total without warning	1,107.62	965.68	
Time to produce warning	145.89	123.15	
Total with warning	1,253.51	1,088.83	
CPU per aircraft without warning (%)	0.029	0.025	12.8
CPU per aircraft with warning (%)	0.033	0.028	13.1
CPU for 64 aircraft without warning (%)	1.86	1.62	12.8
CPU for 64 aircraft with warning (%)	1.83	2.11	13.1

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Table 5

SUMMARY RESULTS OF THE MSAW SIMULATION

	IOP	LSI-2/40	Performance Improvement(%)
CPU utilization per aircraft			
General terrain without warning	0.048%	0.041%	14.4%
General terrain with warning	0.051	0.044	13.1
Primary approach without warning	0.028	0.024	12.9
Primary approach with warning	0.032	0.027	13.3
Satellite approach without warning	0.029	0.025	12.8
Satellite approach with warning	0.033	0.028	13.1
CPU utilization for 64 aircraft			
General terrain without warning	3.07	2.62	14.4
General terrain with warning	3.26	2.82	13.1
Primary approach without warning	1.80	1.57	12.9
Primary approach with warning	2.05	1.78	13.3
Satellite approach without warning	1.86	1.62	12.8
Satellite approach with warning	2.11	1.83	13.1

Table 6

ADDITIONAL CPU LOAD FOR MSAW

	IOP	LSI-2/40
Additional CPU load (percent)		
Tracking	1.4%	1.26%
Common subroutines	0.44	0.40
STPA	0.35	0.31
Data	0.20	0.18
Other*	0.25	0.22
Cumulative CPU utilization for 64 aircraft without warning		
General terrain	5.71%	4.99%
Primary airport	4.44	3.94
Satellite airport	4.5	3.99

Source: Data from ARD-14-8-79, ARTS Performance Measures.

*CYTP, INFC, AUTO, KOFK, TEST.

On an instruction-by-instruction basis, the LSI-2/40 averaged 20% faster than the IOP. Performance can be degraded by as much as 50%, however, in some instruction mixes. The published ARTS III performance measurements indicate that the MSAW module requires 5.6% CPU at a 64-aircraft load. Our computations for the IOP revealed that the CPU requirement at a 100-aircraft load is about 8.1%, including an overhead and safety factor. This produces a per-aircraft CPU utilization of about .0813, which closely parallels the performance of ARTS III. These measurements revealed an increase in performance for the LSI-2/40 in the range of 5 to 10% over the IOP. Overall, a conservative estimate is that the LSI-2/40 is about 5% faster than the IOP in all instruction mixes.

Because no adjustment was made for word size differences between the two machines and no code optimization was performed in the psuedo-conversion technique, these measurements do not reflect a "best case" performance improvement. They are merely the results of executing one particular software design on a faster computer, with no attempt to optimize the design for the architecture of that computer. The results thus probably reflect a worst-case performance improvement.

Overall CPU Capacity Estimates

The approach taken to estimate requirements for CA and the tracker, which is a prerequisite for both MSAW and CA, was different from that used for MSAW. The structure of the code for CA is complex. The program functions are divided into two distinct segments: the primary filter routine and the conflict algorithm routines (proximity, maneuvering, and linear). The latter routines are called only when the primary filter has determined that a particular pair of aircraft are candidates for potential conflict. In evaluating a potential conflict, these routines perform what is probably the most extensive numeric computation in the entire ARTS III system. Also, because they involve determination of the criteria for sensing the conflicts (depending on airport area) and evaluation of several projected positions of the subject aircraft, these routines loop and are nested more than other programs in the system.

The primary filter routine of CA is also very iterative; however, the iteration depends mainly on the number of track pairs available for conflict. To a lesser extent, the primary filter routines depend on the segmentation of airspace and the spatial positions of aircraft and special areas, but the main flow of the filter routine is linear and may be easily estimated.

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Because the conflict algorithm computations represent a signifi-
cant potential for utilization of the computer cycle time, the main
function of the primary filter is to limit the number of times that
these conflict evaluations must be made while ensuring that no poten-
tial conflicts go undetected. This is controlled through parameteriza-
tion of the criteria for filtering and the tuning of these parameters
to achieve acceptable results. The documentation indicates that
acceptable performance may be achieved using parameters that call for
conflict evaluations to be performed on no more than 10% of the
eligible track pairs contained within the system. Because of the
nature of the process for selecting track pairs for evaluation, the
filter routine may pass on to the algorithm routines a certain number
of duplicate pairs (i.e., the same pairs in reverse order). Our
review of ARTS III documentation shows that the performance of the
filter can be adjusted to permit no more than 30% redundant or
duplicate conflict evaluations.

With these levels of performance assumed, the documented methods
of estimating computer utilization can be applied easily for CA in
ARTS III based on the capacity of the ARTS III computer (IOP-B); this
estimate can be validated through performance studies. At a processing
level of 64 tracks, the estimated computer utilization for CA is
approximately 10.1% of an IOP-B.

In the evaluation of MSAW, the analysis of the instruction
timings for the respective ARTS III and ARTS IIA computers had indi-
cated that the estimate of utilization for a given instruction mix
will show a 5% improvement if no regard is given to the fact that cer-
tain arithmetic and data manipulation operations do not operate on the
same amount of data (e.g., the basic addressable unit of storage on
the IOP-B is a 30-bit word, compared with the LSI-2/40 16-bit word).
A careful review of the instruction coding of the ARTS III program

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revealed that in the CA routines, approximately 93.5% of the instruction operations were independent of register capacity. The same review was performed for the tracking and MSAW modules, and approximately 98% and 99% respectively, of the instruction operations fell into this category.

For CA, the remaining 6.5% of the instruction operations must have additional instruction sequences or subroutines used in place of the single ARTS III instructions. This affects the timing for these routines and hence the computer utilization. We assumed that the instructions that needed to be modified were replaced with a sequence taking three times the computer utilization and that the effect of this increased utilization was distributed evenly in the execution of the CA routines. The effects of this adjustment are shown in Table 7.

Table 7

RATIO OF PERFORMANCE BETWEEN THE
LSI-2/40 AND IOP-B

Function	Undegraded Operations	Degraded Operations	Ratio
Tracking	98% @ .95X*	2% @ 3X	.99X
MSAW	99% @ 95X	1% @ 3X	.97X
CA	93.5% @ .95X	6.5% @ 3X	1.08X

*X = IOP speed.

Applying the factor of 1.08 times the estimated computer utilization of 10.1% for CA in ARTS III, we obtained a rounded figure of 10.9% utilization of the computer in ARTS IIA for performance of the CA enhancement.

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This method of estimation allows a conservative margin, considering the following factors:

- The increase in performance due to the cache memory has not been taken into account.

- Code will be optimized for the LSI-2/40 to perform functionally equivalent operations.

- Some operations may be eliminated because of the relaxation of the requirement for the optimization of data storage. This is possible because of the amount of available memory on the ARTS IIA system compared with ARTS III. Examples of this are the masking and unmasking operations required for bit storage, which can be stored as full bytes or words on the LSI-2/40.

- Structured program design methods can be used in ARTS IIA program development. This may yield a more efficient sequence of operations while retaining functional compatibility.

- The capacity requirements for ARTS IIA will most likely be 25% less than the 64 tracks used for computing the estimate.

Applying the same method to the tracking and MSAW programs, a factor of 0.99 in scaling the computer utilization from ARTS III would yield an overall computer utilization of approximately 6.3% for the tracking function and 5.4% for MSAW, also for 64 tracks. Again, this does not take into account any of the considerations for improvement that were itemized for CA and should also yield a conservative figure.

In summary, the requirements of the ARTS IIA computer for the performance of safety enhancement functions could be reliably comparable to the requirements for a single IOP-B running ARTS III. As shown in Table 8, an estimated 22.6% of an LSI-2/40 would be used in performing computations for the safety enhancements for 64 tracks. Other functions, such as display and keyboard functions, will be performed with less efficiency because of differences in the hardware interface and the physical I/O requirements of the system. The limiting factor for system performance on ARTS IIA appears to be similar to that which limits system performance in ARTS II: the system load

Table 8

CPU UTILIZATION ESTIMATES
FOR 64 TRACKS

Enhancement	IOP	Ratio	2/40
Tracking	6.4%	0.99	6.3%
MSAW	5.6%	0.97	5.4%
CA	10.0%	1.08	10.9%
Total	22.0%		22.6%

due to display servicing in a maximum display configuration. The
additional computer power gained by the upgrade of the LSI-2/20 in ARTS
II to the LSI-2/40 in ARTS IIA is sufficient for the additional process-
ing loads of the added enhancement functions, but it will not alleviate
the high load factors due to display overhead.

Assuming that display hardware modification is not economically
feasible, some potential exists for improvement in this area through the
redesign of the functions that build the display data tables.
Currently, the ARTS II function rebuilds the output display data for all
targets on all displays once every quadrant. This results in the
building of display data approximately four times during every scan.
The method used by ARTS III requires only a partial rebuilding of the
display for each quadrant, resulting in complete data building only once
per scan. If this approach were adopted for ARTS IIA, recognizing that
operational differences exist in the display devices, this would help
eliminate the problems of computer saturation during maximum display
loading conditions, which exist when an ARTS IIA system is configured
with more than seven or eight displays.

Given the limits of the ARTS IIA system under maximum display loading, we estimate that the ARTS IIA computer configuration has the capacity to track and perform safety monitoring functions for 50 to 64 aircraft while maintaining and displaying associated and unassociated targets at the same capacity as ARTS II. Loads above this level run the risk of serious degradation of system performance, especially under maximum display loading conditions.

Air Traffic Environment in 1990

Equally as important as determining the additional speed of the LSI-2/40 over the existing ARTS II computer and the CPU requirements of the ARTS IIA safety enhancements was estimating the future air traffic environment of the ARTS II sites. This has been done for the year 1990 using the method described in the Sterling report.[*] The method and data sources used are described fully in Appendix C, and Appendix D presents the computer program used to process the data. Exhibit 7 is a printout from the program of the worst-case--poor weather--air traffic (instantaneous airborne count and associated targets).

Although Exhibit 7 presents both instantaneous targets and associated tartets, only the number of associated targets can be assumed to be accurate. According to the method used, airborne targets accrue from aircraft transiting the radar site area as well as from operations at the site airport. Because of the large number of airports typically within a 60-nm radius of the site, the airborne count cannot be estimated well without data from these (often small) airports. Initial validation efforts for sites from which instantaneous counts were available proved to us that including data for major airports within the radar coverage did not produce the measured number of targets. The numbers in Exhibit 7 for instantaneous airborne count are of the nature of a check for us

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[*]"Assessment of the Capacity of the ARTS IIIA for the Years 1980-1990," Sterling Systems, Inc.

INSTANTANEOUS AIRBORNE COUNT AND ASSOCIATED TARGETS
UNDER POOR WEATHER CONDITIONS IN 1990

PEAK INSTANTANEOUS TARGETS ADJUSTED FOR WEATHER
AND ASSOCIATED TRACKS

22:50 THURSDAY, APRIL 22, 1982   18

YR=90   WTHR=PCOR

ST	SITE	CCDE	TARG_ADJ	IAT
AL	MAXWELL			
CA	EDWARDS	EDW		
GA	ROBINS			
GU	FIH-EGAYA	ZUA		
MA	O.IS	FMH		
OK	FORTSILL			
TX	BERGST-O			
TX	FTHCOD			
LA	FAIRCHIL			
MS	MERIDIAN	MEI	0.2185	0.2076
NY	GRIFFOVE	RME	3.1780	3.0190
CA	PALMSFRG	PSP	3.9326	3.7360
TX	LONGVIEW	GGG	4.7225	4.4063
WY	CASPER	CPR	5.0C30	4.8336
LA	LAKECHAR	LCH	5.8415	5.542?
PA	READING	RDG	6.0913	5.7107
HI	HILO	ITO	6.3458	6.0255
CA	SANTABAR	SBA	7.1319	6.7755
NH	MANCHEST	MHT	7.2741	6.9104
TX	WACO	ACT	7.4077	7.0373
MI	MUSKEGON	MKG	7.4613	7.0583
LA	MONROE	MLU	7.5609	7.1808
MT	MALMCTRO	GFA	7.6537	7.2710
ME	PORTLAND	PWM	7.9491	7.5517
IN	TERREHAU	HUF	7.9840	7.5948
TX	BEAUCONT	BPT	8.0013	7.6018
IA	HATERLOO	ALO	8.1936	7.7744
CO	PUEBLO	PUB	8.2447	7.8325
ME	BANGOR	BGR	8.2509	7.8383
PA	WILKES3	AVP	8.6624	8.2293
FL	FTMEIER	FMY	8.7401	8.3031
OR	EUGENE	EUG	8.9429	8.5014
MO	SPRINGFI	SGF	9.1158	8.6601
MS	GULFPORT	GPT	9.3255	8.8601
NC	WILMINGT	ILM	9.3584	8.8905
AK	FAIRBANK	FAI	9.4239	8.9575
NV	CLARKSBU	CRB	9.7020	9.2169
MN	DULUTH	DLH	9.6942	9.3095
CA	STOCKTON	SCK	9.9652	9.4669
CA	BAKEPSFI	BFL	10.7922	10.2526
IL	CHAMPAIG	CMI	11.7595	11.1716
LA	LAFAYETT	LFT	11.6053	11.0150
NV	RENO	FNO	11.8625	11.2624
MI	KALAMAZO	AZO	12.0439	11.4455
FL	TALLAHAS	TLH	12.1144	11.5087
IA	CEDRRAPD	CID	12.6710	12.0374
NJ	ATLCITY	ACY	12.6750	12.0422
TN	BRISTOL	TRI	13.3513	12.6837
F	CHIPOLA	DFQ	13.4008	12.7307
			13.7551	13.0702
			14.07..	13.5510

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Exhibit 7 (concluded)

PEAK INSTANTANEOUS TARGETS ADJUSTED FOR WEATHER
AND ASSOCIATED TRACKS

YR=90   WTHR=POOR

ST	SITE	CODE	TARG_ADJ	IAT
IL	ROCKFORD	RFD	15.2701	14.5066
MS	JACKSON	JAN	16.1438	15.3366
VA	ROANOKE	ROA	18.1709	17.2623
SC	GREENVIL	GPJ	19.5933	18.6136
AK	ANCHORAG	ANC	20.2239	19.2127
TX	CORPUSCH	CPP	22.6876	21.5533
PA	HARRISB	CXY	24.3137	23.0981
AL	HUNTSVIL	HSV	25.7040	24.4163
VT	BURLINGO	BTV	27.5368	26.1600
GA	SAVANNAH	SAV	28.6684	27.2350
WA	SPOKANE	SKA	29.1188	27.6628
TN	CHATTANO	CHA	29.5653	28.0870
GA	MACONRO3	MCN	30.2401	28.7281
IN	FORTWAYN	FWA	30.2469	28.7345
AL	MOBILE	MOB	30.4370	28.9151
TX	LUBBOCK	LBB	30.8589	29.3444
SC	CHARLEST	CHS	31.2511	29.6886
OH	TOLEDO	TCL	32.6666	31.2252
CO	COLSPRGS	CCS	32.9542	31.3065
IN	SOUTHBND	SBN	33.3797	31.7107
TN	KNOXVILL	TYS	33.7631	32.0750
FL	PENSACOL	PNS	34.5469	32.8195
OH	AKRON	CAK	35.3972	33.6273
VA	RICHMOND	RIC	36.0680	34.2646
AR	LITTROCK	LIT	41.0059	38.9556
KS	WICHITA	ICT	43.1035	40.9493
FL	WESTPBEA	PBI	45.9214	43.6253
NC	GREENSBO	GSO	47.6995	45.3145

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and are not representative of the actual estimated targets. Because the method assumes that associated targets are produced by operations at the site airport, the number of associated targets shown in the exhibit are valid, since data were available for 1979 and estimated for 1990. It is sufficient that these numbers be accurate because the safety enhancement will be applied to associated targets only.

Table 9 shows the number of associated targets estimated for 1990 in poor weather for the eight ARTS II sites with the heaviest traffic. The largest site, Greensboro, is estimated to have 46 instantaneous associated targets (tracks), while only the eight sites in the table have more than 30. It therefore appears appropriate to design the ARTS IIA system for 48 tracks, or a maximum of 64, allowing for error in the method and forecasts.

Table 9

TRACKED TARGETS AT ARTS II SITES
IN 1990 POOR WEATHER CONDITIONS

Site	Instantaneous Tracks
Greensboro	46
West Palm Beach	44
Wichita	41
Little Rock	39
Richmond	35
Akron	34
Pensacola	33
Knoxville	32

VI   SUMMARY AND CONCLUSIONS

This investigation addressed three major questions concerning the proposed ARTS IIA system:

- Can a battery backup system be designed so that memory will be retained during short power failures or fluctuations?

- Is the existing ARTS II code transportable so that the LSI-2/40 can be installed and provide unenhanced ARTS II functions before the ARTS II software has been developed?

- Is the LSI-2/40 fast enough to provide the safety enhancement functions in the expected air traffic environment of 1990?

Regarding battery backup, new devices are being designed now that will be available within the next 6 months. Currently, Computer Automation does not produce an on-memory-board battery or a battery in a power supply that will meet ARTS IIA requirements. Furthermore, if any new power supply with a built-in battery were to be used, modifications of the LSI-2/40 power distribution system would be required to protect memory. External UPS systems are currently available for the application, however, and can be purchased for immediate application with little change to the ARTS system. Fortunately, time is not a constraint; because ARTS II is not currently overloaded and works well, new developments by Computer Automation that may mesh well with ARTS IIA requirements can be awaited without jeopardizing the time schedule for eventual ARTS IIA installation.

The 32K ARTS II tapes can be immediately transferred to and run on the LSI-2/40 computer, but program modification for power-fail-restart will be required. Tapes for 40K ARTS II sites can also be run with minor modifications. The required inclusion of battery backup for memory protection, however, will require additional mouifications

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to both the 32K and 40K systems. These modifications are the same for all ARTS systems (in fact, both 32K and 40K systems can be merged into a single release), and they are not site dependent. Although we reconfigured the tapes on a computer installed in an APC, this can be easily done at FAATC.

Figure 10 indicates the projected percentage of CPU available and the percentage of CPU required for safety enhancements for both 48 and 64 tracked aircraft. Considering the projection of 46 tracked aircraft in 1990 at the busiest ARTS II site, the LSI-2/40 clearly will provide adequate speed for the ARTS IIA system.

No major technical problems exist that would impede the replacement of the LSI-2/20 with the LSI-2/40, simultaneous development of the safety enhancements, and final software changes to the enhanced ARTS IIA system. With appropriate engineering of battery backup as well as well-structured software development, ARTS IIA should become as well regarded as ARTS II is today.
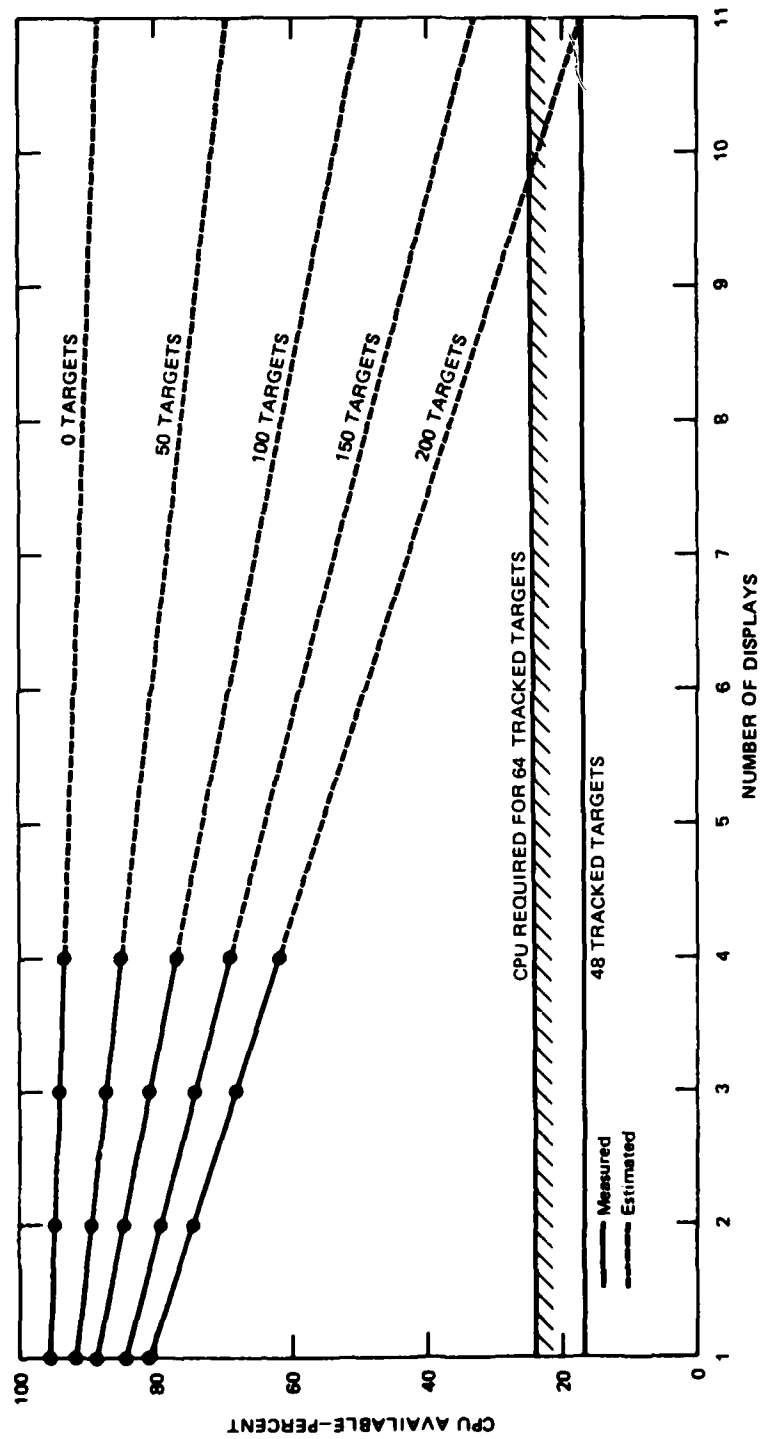
FIGURE 10   LSI-2/40 AVAILABLE WITH 48 AND 64 TRACKED AIRCRAFT

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Appendix A

EXTERNAL BATTERY BACKUP SYSTEMS
OFFERED BY HEWLETT-PACKARD
AND IBM CORPORATION

HEWLETT PACKARD

L-Series Battery backup card

product number 12013A

The 12013A Battery Backup Card provides battery power for sustaining HP 1000 L-Series computer memory during power line outages The batteries, charging circuit, and battery condition signalling circuit are all mounted on the 12013A card, which plugs into a single slot on the L-Series backplane

For a power outage of an hour or less, a fully charged battery backup card will sustain 64k bytes of memory so that the power fail/auto restart capability of the L-Series processor may be used to resume processing Except in the 12032A 5-Slot Card Cage, two 12013A Battery Backup Cards can be used to provide 2 hours of battery sustaining power Sustaining time can be further extended by connecting external batteries

If a long power outage fully depletes the battery charge, the power fail recovery routine will automatically clear memory and will either reboot the operating system or transfer control to the Virtual Control Panel device The 12013A Battery Backup Module can be used with the 12035A Power Module or a power supply designed and built by the user

Features

- 1 hour of sustaining power for 64k bytes of memory on a single L-Series plug-in card
- Up to two battery backup cards can be used in 2103L Computer, 12030A 10-slot Card Cage, or HP 1000 L-Series Model 9 or 10 Computer System
- Audible alarm signals operator when a power failure has occurred and indicates if memory has not been sustained
- Built-in battery charging circuit
- Automatic clearing of memory when power failure outlasts the battery charge
- Connector for external battery pack and remote control of battery backup

Functional specifications

Operational characteristics

Memory sustaining time: At least one hour for 64k bytes of memory when battery is fully charged Two fully-charged 12013A Battery Backup Cards will sustain memory for two hours

Power restart: Detects resumption of power and generates an interrupt to a trap cell for a user-written restart program that has been protected in memory by the sustaining battery

Power control and charging: On-board circuits provide slow charge
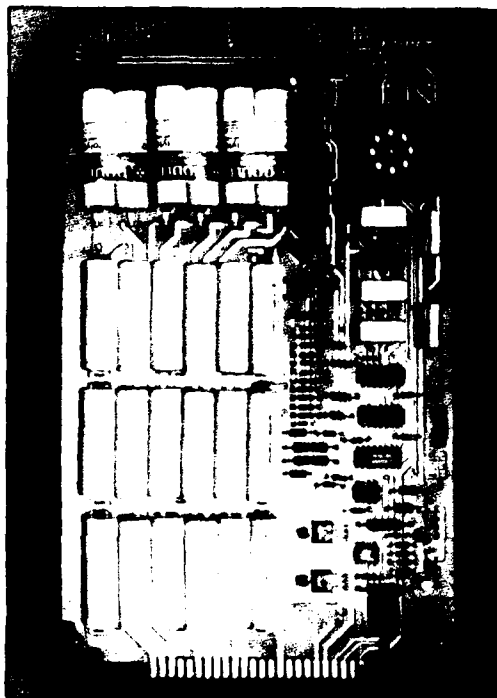
Power fail signalling: A power outage initiates an audible power fail signal that consists of a 1 second beep every 9 seconds while the battery backup module is sustaining memory Resumption of line power or depletion of the battery charge terminates this power failure signal

Reboot signalling: If the batteries fully discharge so that memory has not been sustained the restoration of line power is accompanied by a single two second beep which signals the operator that the system is being or must be rebooted

Remote enable A remote contact closure input on the front printed circuit connector can control whether memory is sustained when power is turned off This can be used to avoid unnecessary depletion of battery charge when it is not necessary to sustain memory

Remote/off/on: A toggle switch provides the following functions

1 Remote, which connects the remote input to the battery backup card control circuits

A-1

2. Off, which disconnects battery sustaining power but permits charging of the backup card batteries while line power is on. This position can be used to prevent unnecessary depletion of battery charge when the computer is intentionally turned off or for battery charging when the computer is not being used.

3. On, which disconnects the remote input from the battery backup control circuits, so the battery backup module always works to sustain memory.

Battery

Type: 1.2 Volt nickel-cadmium cells.

Charging rate: 0.1 of cell capacity rate.

Charge time: Approximately 14 times the total previous discharge time to full charge (14 hours, maximum).

Overload protection: Controlled width traces on the battery backup card function as fusible links which open if 2 to 4 times normal current is drawn from the batteries. Pad eyes are provided on the card for replacement of these links with wire jumpers after correction of an overload condition that causes them to open.

Configuration information

Installation: Because it requires more top-of-card component clearance than other L-Series plug-ins, the 12013A Battery Backup Card should be installed in backplane slot XA1 in the 12032A 5-slot card cage, slot XA1 or XA6 in the 12030A or 2103L 10-slot card cage, or slot XA1 or XA9 in the HP 1000 L-Series Model 9 or 10 System 16-slot card cage.

Number of battery backup cards per computer/system: Maximum of one in 12032A 5-Slot Card Cage, maximum of two in 2103L Computer, 12030A 10-Slot Card Cage, or HP 1000 Model 9 or 10 Computer System. One battery backup card is included in the HP 1000 Model 9 and 10 Computer Systems.

External battery connection: In addition to the remote enable signal traces, front connector traces are provided for connection of external battery power to extend the memory sustaining time of the battery backup card.

One battery backup card and a mating connector that can be used for connection of an external battery to the battery backup card is included with HP 1000 Model 9 and 10 Computer Systems, but such connection will require additional wiring to that mating connector. For use with 2103L and 2103LK Computers, a 48-pin connector kit, HP Part Number 5061-3426, provides the required mating connector.

Electrical characteristics

Direct current requirements

170mA(+12V), 10mA(−12V)

Physical characteristics

Dimensions, mm (and inches)

289 (11.38) long

172 (6.75) wide

17.8 (0.7) Parts clearance

Board thickness 1.6 (0.063)

5.1 (0.2) Beneath board clearance
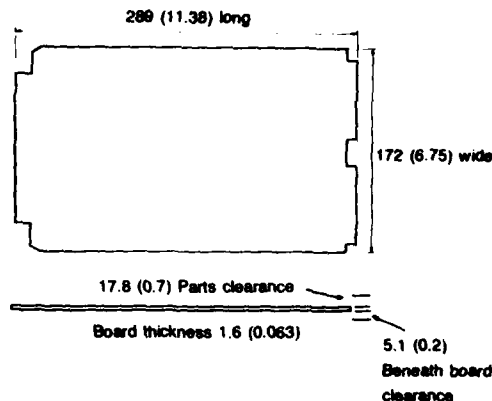
Weight

909 grams (2 lb)

Ordering information

12013A Battery Backup Card

NOTE: One 12013A Battery Backup Card is included in HP 1000 L-Series Computer Systems, Models 9 and 10.

Power fail recovery systems for HP 1000 computers and memory extender

models 12944B and 12991B

The 12944B and 12991B power fail recovery systems provide battery sustaining power for memory during line power outages, as well as battery charging circuitry, and battery charge state testing. If a line power outage does not last long enough to deplete available battery charge, the power fail auto restart feature of HP 1000 computers may be used to resume processing. If, on the other hand, a line power outage lasts long enough to deplete available battery charge the power fail recovery system prevents automatic power up and signals the operator that this condition exists

Features

- Sustains memory through power failures
- Tests battery charge state and provides a low battery warning indicator
- Provides automatic memory clear on power failures lasting longer than available battery charge
- Operates throughout the entire range of HP 1000 environmental specifications

12991B power pack mounted on rear of 2113 Computer

Functional specifications

Application

12944B is used for battery backup of 2108M and 2109E Computers. It contains one 14-volt sealed lead-acid battery with a rating of 5 ampere-hours.

12991B is used for battery backup of 2111F, 2112M, 2113E, and 2117F Computers and 12990B Memory extenders. It contains two 14-volt sealed lead-acid batteries, each with a rating of 5 ampere-hours.

Memory sustaining time

No. of mem. modules:	1	2	3	4	5	6	7	8	9	10
Hours with 12944B:	41	33	25	19	16					
Hours with 12991B:	44	38	34	30	26	23	22	21	20	18

Power restart

Detects resumption of power and generates an interrupt to trap cell for user-written restart program which has been protected in memory by the sustaining battery

Power control and charge unit

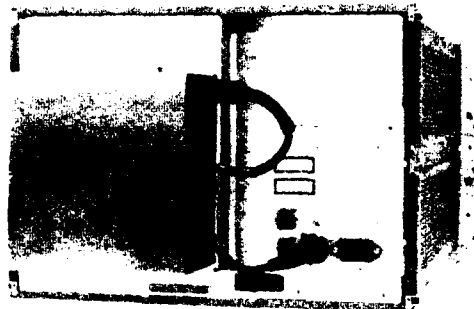Monitors battery charge status and provides slow charge

Sustaining battery

Type: 14 volt, 5 amp-hr (12944B) or 10 amp-hr (12991B) sealed lead acid

Charging rate: 2A, maximum

Battery charge time

Approximately 16 hours to fully-charge

Installation

To install, secure the battery pack to the back of the computer or memory extender, plug the printed circuit cards into the power supply, and connect the battery cable to the extender's input battery connector

Physical characteristics

12944B: Adds 11.1 cm (4-3.8 in) to overall depth, 4.3 kg (9.5 lb) to weight of the Computer

12991B: Adds 11.1 cm (4-3.8 in) to overall depth, 7.3 kg (16 lb) to weight of the Computer or Memory extender

Ordering information

12944B power fail recovery system

The 12944B power fail recovery system includes
1 12944-60001 battery pack
2 5061-1348 battery charging assembly
3 5061-1349 battery backup assembly
4 12944-60002 cable
5 12944-90005 installation manual

12991B power fail recovery system

The 12991B power fail recovery system includes
1 12991-60001 battery pack and mounting hardware
2 5061-1348 battery charging assembly
3 5061-1349 battery backup assembly
4 12944-60002 cable
5 12991-90004 installation manual

The 4999 unit provides the 4952 (Model B only) and 4955 Processors with emergency ac power when utility power is inadequate or temporarily lost. The 4999 is available in two models based on the operating voltage of the processor:

    Model 1—for 100—123.5 volts ac, 60 Hz power
    Model 2—for 200—240 volts ac, 60 Hz power

Both models mount in one half-width of an IBM 4997 Rack Enclosure or EIA standard rack enclosure by means of the Rack Mounting Fixture (feature number 4540).

Utility power is supplied to the Series/1 processor through connections on the 4999 unit. Primary power is monitored by the unit, and in the event of a power dip or failure, the input power to the battery backup unit is automatically switched to 12-volt battery power. The battery and battery charger unit are supplied by the user. The battery power is inverted from dc to ac and supplied to the processor as square-wave ac power at the required voltage level.
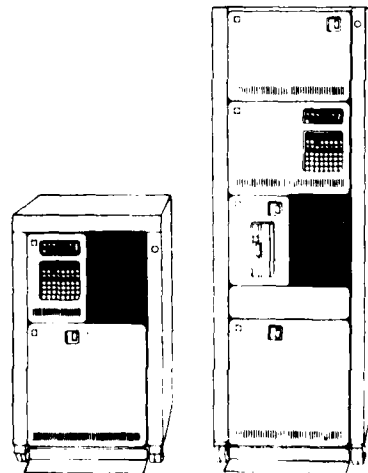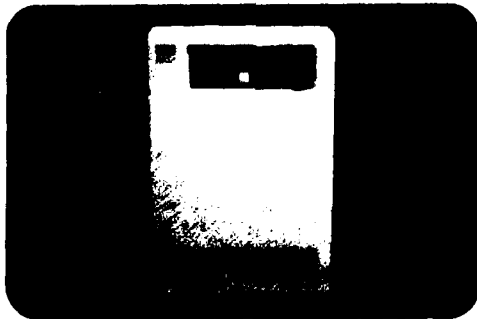
Appendix B

UNINTERRUPTIBLE AC POWER SOURCE
OFFERED BY DELTEC

Deltec, a member of the Power Conversion Division of Gould, Inc., is the designer and manufacturer of solid state power conversion equipment in the low and medium power ranges. Deltec offers the most extensive line of products to solve AC power problems of every type — blackout, brownout, changing voltages and electrical noise. Because of this broad capability, Deltec can offer the most cost effective solution to AC Power problems. Over 2,000,000 VA of static inverters and uninterruptible power systems are in use today.

DSU Series Uninterruptible Power Systems (UPS) offer the ideal solution for backing-up small business computers, PABX, process control, monitoring and data acquisition and machine control systems. They are designed for rack mounting with modular circuit assemblies for maximum MTBF and minimum MTTR.

Deltec's new "20" Series UPS is an improved version of the time-tested DSU product line of which there are over 1000 units in operation today. The "20" Series incorporates the latest technology and designs in order to further enhance reliability and maintainability.

The basic power train and operation is similar to our original DSU systems thereby maintaining the history of qualified operation with computer systems manufactured by such companies as Digital Equipment Corporation, Hewlett Packard, Wang Laboratories, and Data General.

The Basic "20" Series

The basic "20" series provides the most economical approach to a full UPS for small computer process control systems. One of these units with a single RP10 or RP20 battery reservoir pack will provide on-line, clean, stable, no break power during short term utility power interruptions.

Included is a direct line rectifier, battery charger and a highly reliable sine wave static inverter. Also included are battery charger controls, frequency and alarm controls, remote contact closures, output voltmeter and ammeter, LED status panel and an electro-mechanical break-before-make reverse transfer switch.

A complete range of battery reservoirs are available for mounting internally or externally to provide back-up power ranging from 5 minutes to over 4 hours depending on your particular equipment power requirement and the application.

For those who wish to use wet cell or nickel cadmium batteries which would be mounted on an open rack, a 1:1 isolation transformer can be incorporated in the DSU at additional cost. This provides AC to DC isolation required for safe, hazard-free operation.

Should the standard electro-mechanical transfer switch time of approximately 20 milliseconds be incompatible for your application, the state of the art, DSS2001 Static Transfer Switch is available. This provides a maximum of 4 millisecond sense and switch time and make-before-break operation. The system automatically senses overload and transfers the load to bypass at 130% of nominal full load. When the overload reduces to 105% of nominal, the load is automatically returned to the inverter. This will permit the start-up of disk drives without requiring a larger UPS.

Unlike many manufacturers, Deltec has recognized the problems caused by Radio Frequency Interference and Electromagnetic Interference (RFI EMI). If the application includes a special consideration for conducted RFI EMI qualifications, an RFI EMI filter can be ordered. These applications occur in some installations with communications equipment or when providing power to certain mini or micro computer systems.

A NEMA 1 enclosure, ENC-20, is available which can accommodate the DSU, the DSS2001 Static Transfer Switch and up to three RP20 battery reservoir packs.

Applications

Data Processing

The DSU is compatible with small Data-Processing systems and is desirable because of its easy installation, lack of required periodic maintenance, and ease of service, if required.

Telecommunications

UPS back-up for PABX systems eliminates the "lost" customer due to a power glitch or power break. With a minimum back-up system, phone calls can be orderly terminated should a major blackout occur. If your telephone is the most important communication link of your business, additional reservoir time can be ordered to allow continued operation in an excess of one hour.

Process Control

DSU's are widely used in mini micro control systems, set-point controllers and data acquisition systems. This minimizes the investment for clean, stable power within a facility where such quality power was not previously required.

Medical Industry — backup of critical biological testers and life support systems such as heart-lung machines.

Security Systems — backup of fire intrusion/disaster alarm systems to provide continuous monitoring even in the event of a utility power failure.

Banking Industry — backup of Automatic Teller Machines to avoid users' ill-will which results when their identification cards are retained by the ATM in the event of a power failure.

Machine Tool Industry — backup of cost-critical computerized machine tools and metal-forming equipment to avoid damage to the machine itself or to the piece part.

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Specifications

Performance

Input

120 VAC ± 10%, 57-63 Hz (50 Hz available)

Output

120 ± 2VAC
Regulation: ± 3% line and load
Frequency: 60 Hz ± 0.5% *(50 Hz available)*
Waveform: Sine wave, maximum 5% harmonic distortion full load.
Power Factor: *0.8 lag to unity*
Meters: AC voltage and AC current
Overload: 25% over nominal for 15 minutes

General

Controls: AC input "On-Off" DC input (to inverter) "On-Off"

Indicators: LED-AC Input present (green), Battery Recharging (amber), Battery Low (red), Load On Bypass AC (amber)

Transfer Switch: Electro-mechanical transfer, break-before-make, 20 milliseconds. 4 millisecond static transfer switch available

Recharge to Discharge Ratio. 10 to 1

Operating Temperature: 0°C to 40°C *(50°C available) (Batteries rated at 25°C)*

MTBF: Greater than 20,000 hours, unit, greater than 100,000 hours, system

MTTR: Approximately 30 minutes

Remote Contact Closures: Dry relay contacts, loss of AC input, loss of inverter output, battery low — approximately 1 to 2 minutes before shutdown, overtemperature, (load on bypass with DSS2001 only)

Table 1
Unit Specifications

	DSU720	DSU721	DSU1220	DSU1221	DSU1820	DSU1821
Input Isolation Transformer*	No	Yes	Yes	Yes	No	[illegible]
Input						
Current (max) Amps	10.5	11.5	18.0	21.4	[illegible]	[illegible]
Connection	Terminals		Terminals		Terminals	
Output						
Power	700VA		1200VA		1800VA	
Connection	Terminals		Terminals		Terminals	
Package						
Front Panel Height (in.)	10.480		[illegible]		[illegible]	
Chassis Height (in.)	10.195		[illegible]		[illegible]	
Front Panel Width (in.)	19		19		19	
Chassis Width (in.)	17		17.125		17.125	
Depth (in.)	21		21		21	
Net Weight (lbs.)	115**	140**	160	180	180	[illegible]

*If using external batteries mounted in open frame rack(s) a model incorporating the input isolation transformer is required to eliminate potential shock hazard

**Does not include available internal RP 10 Battery. If ordered, add 30 lbs

Options

DSS 2001 Static Transfer Switch.

The DSS is a make-before-break, solid state static reverse transfer switch with an LED status display. The switch protects against power breaks to the critical load due to equipment failure or due to heavy overloads during equipment start up or load branch failure.

Transfer time: 1 ms
Total Sense and Transfer Time: 4 ms
Overcurrent Capacity: 125% for 20 sec, 200% for 4 sec
Remote Contact Closure: Closes when load has been transferred to bypass
Manual Transfer Switch
Physical Characteristics
Rack Mount 19" Rack Mount 5 219" H
Weight 15 lbs

Isolation Transformer. Space inside the DSU has been provided to incorporate the optional 1:1 input isolation transformer. This is required to prevent shock hazards when the DSU is used in conjunction with wet cell or nickel cadmium batteries installed on open frame racks.

Battery Reservoir Pack (RP). Table 2 indicates back-up times available for different power levels and different load percentages

Nickel Cadmium Battery Charger Control Board. This board is to be ordered whenever the DSU is used with nickel cadmium batteries. The board automatically provides float voltage to the batteries and switches to high-rate charge whenever triggered due to battery discharge during a utility power interrupt. The board mounts in place of the standard battery charger control board.

RFI/EMI Filter. If it is determined *that special filtering considerations are* necessary based upon the application, such filtering should be ordered at the same time as is the DSU. The filtering unique in the small power ranges addressed by the DSU, is mounted inside of the DSU to provide optimum performance without affecting nearby sensitive electronic equipment.

ENC-20 Enclosure. A free standing, fork-lift base, NEMA 1 enclosure is available. It can accommodate a DSU, a DSS2001 and up to three RP packs. All interconnect wiring is done at the factory thereby providing a total system ready for customer input and output wiring.

Physical Characteristics
Size: 52 25"H x 22 16"W x 30 88"D
Weight: Approximately 125 lbs

Table 2 Battery Characteristics

Model	DSU720 700VA			DSU1220 1200VA			DSU1820 1800VA		
% of Nominal Load	50%	75%	100%	50%	75%	100%	50%	75%	100%
RP10 (internal to DSU720)	15min	8min	5min	Not applicable			Not applicable		
RP20 1 Unit	120min	87min	60min	[illegible]	34min	[illegible]	[illegible]	20min	[illegible]
2 Units	[illegible]	[illegible]	[illegible]	140min	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
3 Units	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	140min	[illegible]	[illegible]
[illegible]	RP20 Unit (rack mounted)								
	Front Panel Dimensions in Inches			[illegible]					
	Chassis Dimensions in Inches			[illegible]					
	Net Weight (lbs.)			[illegible]					

GOULD
DELTEC

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SECTION IIIA

DELTEC UNINTERRUPTIBLE POWER SYSTEMS

DSU "20" SERIES

1.0   GENERAL DESCRIPTION

The Deltec Uninterruptible Power System (UPS) affords the
user uninterrupted, transient-free power based on
battery reservoir energy. Batteries are available which
provide from five minutes to four hours of standby energy,
depending upon UPS size and load percentage. The size
of the DSU series is well-suited to mini-computer based
systems and to other electronic systems which require
continuous, quality AC power to prevent equipment damage
as well as ineffective and unreliable operation commonly
caused by blackouts, brownouts, and transients.

Independent surveys from different areas of the United States
show that on an average: utility power failures or severe
brownouts occur less than .1% of normal operation time,
are less than five minutes duration, and occur on an
average of two to three per month. Obviously to the
computer user, there are many variations of these averages.
These figures do not include weather or customer caused
interruptions, brownouts, and transients. A lightning
strike close to a user will cause power interruption not
recorded at the utility facility or by other customers.

A UPS installation appears straightforward and uncompli-
cated; however, successful and reliable UPS installations
have proven to be more difficult in practice. Difficulties
generally occur due to lack of knowledge concerning
critical equipment requirements, fault clearing, motor
start surges, and other such peculiarities of the system
"Power Profile".

Deltec UPS installations have achieved the goal of
providing quality power with the maximum degree of
reliability at an economical life-cycle cost. Deltec has
demonstrated rapid and reliable delivery performance with
the maximum of reliability and suitability to the applica-
tion. References are available on request.

Deltec systems utilize the latest state-of-the-art standard
solid-state devices. Low level circuits, i.e., oscillator
drivers, sensors and control logic, employ MSI and other
integrated circuits mounted on easily accessible plyg-in
boards. All power components are silicon type. Power

Silicon Controlled Rectifiers (SCR's) and rectifying
diodes are employed at a rating of 1/3 or less of
their specified capability. All components are
standard and available at national distributors.

The UPS is assembled with standard relay-rack mountable
panels for easy "plug-in" installation. The entire
system is sequenced, tested, and operated for at
least 16 hours at Deltec. Installation requirements
are minimal and can be accomplished by an electrician
or electronic technician.

All systems are configured as reverse transfer systems.
This means that the critical load is continually
powered by the UPS system. Should the utility AC line
fail, there are no switching or other transients whatsoever.

2.0   SYSTEM DESCRIPTION

2.1   General Configuration (see Figure 1)

A Deltec DSU Series UPS System consists of a phase-
controlled SCR Power Rectifier/Battery Charger, a Power
DC/AC Static Inverter, protective and convenience circuit
breakers, a convenience manual transfer switch and LED
status indicator lamps paralleled with dry relay contact
closures which are available for remote monitoring.

Various options are available. Please refer to Paragraph
3.0.

All DSU components are included in one rack-mountable
console. The DSU series is designed to be installed
between present electrical power input systems and the
critical load without special wiring or fixtures.

The basic unit will drive the specified critical load
during short term power failures. The backup power
capability is governed by the battery reservoir pack (RP)
and will be specified based upon the specific application.
See Paragraph 3.2.

2.2   Operation

During normal operation, power is derived from the utility
bus and is fed through the AC input circuit breaker to the
Power Rectifier/Battery Charger. The Power Rectifier
converts the AC to DC which is fed through the DC input
circuit breaker to the Static Inverter input and the
Battery Reservoir. The Battery Charger maintains the

reservoir at full energy level. The Static Inverter
supplies NO-BREAK AC power to the critical load.

Should a utility power failure occur, the battery reservoir
automatically supplies DC energy to the Inverter. There
is no switch or other relay changeover, and therefore, there
are no transients of any type created on the AC output.
The front panel AC Input LED extinguishes and a dry contact
closure is initiated, indicating the utility failure.
These signals can be used to activate alarms or other
devices locally or remotely.

The inverter normally drives the critical load. Should
an unexpected system failure occur, the electromechanical
manual transfer switch will automatically switch the load
to bypass AC power and illuminate an amber LOAD ON BYPASS
AC LED thereby providing power to the load even in the un-
likely event of DSU failure. This electromechanical break-
before-make switch operates in 20-50 milliseconds, and
switches the critical load from the inverter to the bypass
AC line if the inverter output voltage drops below 90-95%
of nominal. A contact closure also activates.

2.3   Control Panel

2.3.1   General

The control panel and meters (AC output voltage and current)
are designed to allow ease of system monitoring by personnel.
All controls and indicators are located on the front panel
for convenience of operation.

2.3.2   Description of LED Indicators and Contact Closures

Dry, normally open contact closures are provided for use with
remote monitors, alarms, or other devices. These are
accessible at a terminal strip mounted at the rear of the
unit. Contacts are rated at 2 amps resistive, 120VAC/28VDC.

LED INDICATOR	CONTACT CLOSURES
2.3.2.1 AC INPUT - Green LED	NO AC INPUT
When illuminated, indicates AC Input circuit breaker is closed and AC power is available to the UPS.	Contact closes when AC Input circuit breaker is closed but no AC power is available.

	LED INDICATOR	CONTACT CLOSURES
2.3.2.2	BYPASS OUTPUT - Amber LED	NO INVERTER OUTPUT

2.3.2.2   BYPASS OUTPUT - Amber LED   NO INVERTER OUTPUT

When illuminated, indicates that the load is operating from bypass AC power. This transfer will occur automatically if the inverter malfunctions or if the Transfer Switch has been actuated.

Contact closes whenever the load is operating from bypass AC power.

2.3.2.3   BATTERY ALARM - Red LED   BATTERY LOW

When illuminated, indicates the battery is below 63.5 V $\pm$ .5 V and the system will shut down in approximately 1-2 minutes.

Contact closes when the battery is below 63.5 V + .5 V indicating that the system will shut down in approximately 1-2 minutes.

2.3.2.4.   BATTERY RECHARGE - Amber LED

When illuminated, indicates charging current to the batteries.

2.3.2.5   OVER TEMPERATURE

Contact closes when the temperature of the inverter heatsink exceeds 82°C.

3.0   OPTIONS

3.1   Static Transfer Switch

In the event that Manual Transfer Switch switchover time of 20-50 milliseconds is excessive, the standard electromechanical transfer switch can be replaced with a Static Transfer Switch, which senses the loss of normal inverter output and switches to bypass power in a total of less than 4 milliseconds (¼ cycle). In addition, it also senses current overload and automatically transfer the load to bypass if current exceeds 30% of nominal. Once the overload is reduced to approximately 105% of nominal, the load will be automatically returned to the inverter. An LED will be illuminated on the front panel to advise personnel of such action and a contact closure is activated. The switchover requires manual reset to restore the load to the inverter if the transfer was due to inverter failure.

Since the Static Transfer Switch is make-before-break,
frequency synchronization between the inverter output and
the bypass AC line are necessary and is provided. The
static switch front panel has LED Indicators to indicate
if the load is being driven from the inverter (green LED)
or from the bypass AC line (amber LED), if overcurrent is
being sensed (red LED) and if the inverter output and the
bypass AC are in phase (green LED). A manual transfer
switch and an AC Output circuit breaker are also provided.

3.2   Battery Reservoir

A complete range of battery reservoirs are available for
mounting inside the DSU or external to it. They can provide
back-up power ranging from 5 minutes to over 4 hours depend-
ing upon your particular power requirements and application.

The most common reservoir consists of maintenance free,
gelled electrolyte batteries and are available in the two
configurations, RP10 and RP20. The RP10 is available as an
internal reservoir pack for a 700VA DSU only. The RP20 is
configured as rack-mountable, enclosed modules providing
various back-up times relative to the model of DSU and to the
percentage of load.

Back-up times are as follows:

	DSU 720-700VA			DSU 1220-1200VA			DSU 1820-1800VA		
Percentage of Load	50%	75%	100%	50%	75%	100%	50%	75%	100%
RP10 (Internal to DSU 720)	12min	7min	5min	Not Available			Not Available		
RP20: 1 Unit	120min	75min	50min	50min	35min	15min	30min	20min	10min
2 Units	290min	200min	130min	145min	85min	60min	80min	55min	35min
3 Units	480min	300min	260min	260min	160min	110min	30min	90min	65min

3.3   Input Isolation Transformer

In the event that greater back-up times are required than
can be achieved with the RP's or if a particular applica-
tion dictates the usage of wet cell batteries (lead-cal-
cium or nickel cadmium), an input isolation transformer
will be required to prevent shock hazards when using
batteries on open frame racks. The input transformer will
be mounted internally in the DSU and is specified by choosing
the appropriate DSU model number, eg. DSU 720 - without
input isolation transformer, DSU 721 - with input isolation
transformer.

3.4   RFI/EMI Filter

If it is determined that special AC filtering considerations
are necessary due to the application, such filtering should
be ordered with the DSU and is mounted internally. Radio
Frequency Interference and Electromagnetic Interference
RFI/EMI) can potentially degrade overall site performance
in some communication installations or when driving certain
mini or micro computer systems.

3.5   ENC-20 Enclosure

A free standing NEMA 1 enclosure is available to accomodate
a DSU, a Static Transfer Switch and up to a maximum of three
RP20 modules. Components are shipped installed and inter-
connected ready for customer supplied input and output wiring.

4.0   COMPONENT DESCRIPTION AND OPERATION

4.1   Power Rectifier/Battery Charger

4.1.1   Description

The SCR Power Rectifier/Battery Charger is a full-wave
rectified SCR bridge. Sense and control circuits are
modular-constructed printed circuit boards which are
accessible for service or replacement.

4.1.2   Electrical Specifications

INPUT

    Voltage: 120VAC + 10%, single phase
                             57 - 63 Hz

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Current:	DSU 720 - 15 amps
(Full load and	
maximum charge	DSU 1220 - 26 amps
conditions,	
nominal line)	DSU 1820 - 38 amps

OUTPUT

Float Voltage:	84VDC
Current Limit:	Factory adjusted to protect batteries

4.2   Power Static Inverter

4.2.1   Description

· The all-silicon crystal-controlled oscillator drive
system is designed on a modular plug-in circuit board.

The inverter SCR's are designed to provide continuous
reliable power. Extensive evaluation of SCR's allows
Deltec to use devices which are specified to provide
200% to 300% more power than the required nominal
output. Fast SCR's coupled with snubber circuits
provide long life, no-misfiring operation. Snubber
circuits also suppress common SCR-caused RFI spikes.

The output ferroresonant transformer, designed and
manufactured at Deltec provides the most reliable
inverter output method available. This saturated
magnetic system is insensitive to full step input
changes over the specified range. Filter chokes
provide harmonic suppression of the output signal,
which is a computer-grade sine wave. The inherent
current limit feature of this system provides short
circuit protection. The energy storage of the
output transformer and resonant capacitor provides
the capability to start AC motors with in-rush
currents of up to 300% of inverter specified output
current.

4.2.2   DC/AC Static Inverter Electrical Specifications

INPUT

Voltage:	84VDC (float voltage)

OUTPUT

Voltage:	1∅, 120VAC ± 2VAC
Voltage Regulation:	± 3% no load to full load and varying input

Frequency:	60Hz ± 0.5%		
Harmonic Distortion:	5% maximum at full lo.		
Current (Maximum):	DSU 720 – 5.8 amps DSU 1220 – 8.3 amps DSU 1820 – 15.0 amps		
Overload Capability:	125% of nominal (would *decrease* battery backup time if running off of battery reservoir)		
Power Factor:	0.8 lagging to unity		

5.0 ENVIRONMENTAL

AC to AC Efficiency:	68% at full load
Audible Noise Level:	Less than 68dBA at 5 feet
Operating Temperature:	0 to 40°C. Cooled by forced air
Non-Operating Temperature:	– 20 to + 70°C.
Altitude:	10,000 feet above sea level
Relative Humidity:	0 to 95% noncondensing

6.0 DIMENSIONS AND WEIGHTS

6.1 DSU Cabinet

All models are rack mountable. Due to their weight, DSU's are to be supported by mounting brackets and not by their front panels.

	700VA	1200VA	1800VA
Front Panel Height (in)	10.469	13.969	13.969
Chassis Height (in)	10.125	13.625	13.625
Front Panel width (in)	19	19	19
Chassis Width (in)	17	17.125	17.125
Chassis Depth (in)	21	21	21
Net Weight – "20" Series* (lbs)	115**	150	183
Net Weight – "21" Series* (lbs)	140**	190	237

* "20" Series has *no* input isolation transformer; "21" Series does.

** Weight does not include available RP10, 5 minute internal battery reservoir. If RP10 is ordered, add 30 pounds for total weight.

Appendix C

ESTIMATION OF INSTANTANEOUS ASSOCIATED TRACKS
FOR ARTS II SITES IN 1990

ESTIMATION OF INSTANTANEOUS ASSOCIATED TRACKS
FOR ARTS II SITES IN 1990

The method of estimating peak instantaneous associated tracks at
ARTS II sites described here was based on the method developed in the
report, "Assessment of the Capacity of the ARTS IIIA for the Years
1980-1990," prepared for the FAA by Sterling Systems, Inc. (Refer in
particular to pages A-18 through A-30 of the Sterling report.)

The method is coded in SAS, a computer language and system for
performing data processing and statistical analysis. Appendix D is a
copy of the SAS program.

The method is based on the following premise: At ARTS II sites,
associated tracks are created for aircraft performing instrument
operations within range of the sensor. Each such operation is counted
as an instrument operation in FAA statistics for the co-located
airport. The converse is also assumed: All instrument operations
counted at the co-located airport give rise to an associated track,
provided the aircraft is suitably equipped.

In view of this, the peak instantaneous count of associated
tracks in 1990 at a given site can be estimated using as primary input
the FAA forecast of instrument operations at the co-located airport
for 1990 presented in the FAA document, "Terminal Area Forecasts."
(This source is refered to as TAF.)

Average operation counts are converted to average instantaneous
target counts by multiplying the former by a number that represents
the average length of time that a given aircraft counted as an
operation is detected as a target. This time varies considerably

among aircraft performing different types of operations and having different capabilities. For example, according to the Sterling report, general aviation and air taxi or commercial aircraft performing instrument operations in the vicinity of an airport are under control about 25% longer than air carrier or military aircraft. Thus, among airports with an equal number of instrument operations, the number of beacon targets will be greater at the airport with the greater proportion of general aviation. Consequently, a breakdown of the forecast between various activity categories is developed before the total target count is determined.

The estimate of peak instantaneous associated tracks can be produced through the following four steps, which correspond to three DATA steps and a PROC SUMMARY step of the SAS procedure:

(1)   Break down the forecast for 1990 of instrument operations at an ARTS II site into the carrier categories of air carrier, military, and a group consisting of air taxi, commercial, and general aviation. Estimate the ratio of peak-hour instrument operations to average-hour instrument operations.

(2)   Convert average operation counts by carrier category to peak instantaneous target counts.

(3)   Summarize the results over carrier category to obtain total peak instantaneous target counts by site.

(4)   Apply assumptions about the number of associated tracks generated by a given number of targets. Apply assumptions about weather.

These steps are described in the following paragraphs.

Estimate Average Annual Activity Levels by Activity Types and Busy/Average Hour Ratio

Air Carrier and Military Instrument Operations--Air carrier and military instrument operations for the base year at an airport are obtained from Table 9 of FAA Air Traffic Activity, Fiscal Year 1979.

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The estimate for 1990 air carrier instrument operations assumes the same growth rate as that experienced by air carrier operations in general. Air carrier operations for the base year and for 1990 are obtained from TAF. Military instrument operations are assumed to remain at the same level as during the base year.

Other Instrument Operations—Other instrument operations (air taxi, commercial and general aviation) are the difference between estimated 1990 total instrument operations (from TAF) and estimated levels of air carrier and military instrument operations obtained above.

Busy/Average Hour Ratio—The busy/average hour ratio, BAR, is obtained from a regression formula developed in the Sterling report:

$$BAR = 2.51 \exp (-.001 \ x) + 1 \quad ,$$

where x is the total instrument operations in thousands estimated for 1990 (from TAF).

Convert Annual Activity Levels to Peak Instantaneous Target Counts

The typical air carrier or military aircraft performing an instrument operation in the vicinity of a sensor is assumed to be a target for 0.2817 hour (̇ ̇ ̇ut 16.9 minutes). The remaining aircraft are assumed to be targets for 0.3482 hour (about 20.9 minutes). These factors are based on an analysis of hypothetical flight paths and some additional assumptions in the Sterling report (see pages A-23 and A-24 and Appendix F).

Average annual activity levels are converted to average hourly activity levels by dividing by 8,760 (the number of hours in a year), then to peak hourly activity levels by multiplying by BAR, and then to instantaneous target counts by multiplying by the appropriate conversion factor. The result is the average target count that will be

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observed during the peak hour. This is multiplied by 1.2 to obtain
the peak instantaneous target count (see page A-24). After this
computation, the result is summarized over carrier category.

Apply Track-to-Target Ratio and Weather Assumptions

The foregoing two steps produce the peak instantaneous number of
aircraft receiving instrument flight control from the site. According
to the Sterling report (page A-25), it is assumed that 95% of these
aircraft are equipped for Mode C and will be assigned a discrete code
and that the entire 95% will therefore be in associated track status.
Because peak instrument operations occur during poor weather, the
result (.95 times the number of targets) is the poor weather estimate
of peak associated tracks. Good weather associated tracks are assumed
to be 75% of the poor weather values.

Appendix D

SAS COMPUTER PROGRAM USED TO ESTIMATE
ARTS II AIR TRAFFIC IN 1990

```
1.      //TRACK JOB (C22$W2),'DESOPD SRI - BN!11'
2.      // EXEC  SAS,OPTIONS='NOOVP,NOCENTER'
3.      //SYSIN DD *
4.
5.      *  NOTE: IN THE FOLLOWING, PAGE NUMBER REFERENCES ARE TO
6.         THE STIRLING REPORT;
7.
8.      PROC FORMAT; VALUE CARF 1=ACAR 2=MIL 3='AT+CM+GA';
9.      PROC FORMAT; VALUE WTHRF 1=GOOD 2=POOR ;
10.     PROC FORMAT; VALUE YEARF 1=79 2=90;
11.
12.     DATA ACTLEV;  *  CONVERTS INPUT LINES TRANSCRIBED FROM TRAFFIC
13.                      ACTIVITY LEVELS AND FORECASTS TO ACTIVITY LEVELS
14.                      BY TYPE OF CARRIER  ;
15.
16.       INPUT ST $ SITE $ CODE $ INAC79 INML79 INTOT79
17.               OPAC79 IN79 OPAC90 IN90;
18.       KEEP ST SITE CODE YR CAR_TYP ACT_LEV BAR;
19.
20.       BAR = 2.51*EXP(-.001*IN90)+1;
21.       IF OPAC79 ¬= 0 THEN RTO = OPAC90/OPAC79; ELSE RTO=1;
22.       INAC90 = INAC79*RTO;
23.       INML90 = INML79;
24.       INTOT90 = IN90*1000;
25.       ARRAY INAC(I) INAC79 INAC90;
26.       ARRAY INML(I) INML79 INML90;
27.       ARRAY INTOT(I) INTOT79 INTOT90;
28.
29.       DO I = 1 TO 2;
30.         YR = I;
31.         CAR_TYP = 1;  * AIR CARRIER;
32.         ACT_LEV = INAC;
33.         OUTPUT;
34.
35.         CAR_TYP = 2;  * MILITARY;
36.         ACT_LEV = INML;
37.         OUTPUT;
38.
39.         CAR_TYP = 3;   * AIR TAXI PLUS GEN. AVIATION;
40.         ACT_LEV = INTOT - INAC - INML;
41.         OUTPUT;
42.       END;
43.
44.       * -------------------INPUT LAYOUT----------------------------;
45.       *
46.                          INAC  INML  INTOT OPAC IN OPAC IN
47.       ST SITE     CODE    79    79    79   79  79  90  90
48.       -- ----     ----   ----  ----  ----- -- --- -- ---;
49.       CARDS;
50.       AK ANCHORAG ANC    59362 29085 131939 55  90  72 155
51.       AK FAIRBANK FAI    10906  2550  17738 14  42  18  62
52.       AL HUNTSVIL HSV    18565  7771 118215 18 120  23 180
53.       AL MAXWELL    .      .     .      .    .   .   .   .
54.       AL MOBILE   MOB    20361 18975 124531 23 144  28 220
55.       AR LITTROCK LIT    28920 41362 202457 26 213  32 319
56.       CA BAKERSFI BFL     4589  1062  40685  7  45   9  69
57.       CA EDWARDS  EDW     6407 128514 167974  .  .   .   .
58.       CA PALMSPRG PSP     9660  1522  27642 10  18  15  27
59.       CA SANTABAR SBA     3918   166  37350  6  29   8  45
60.       CA STOCKTON SCK     5264  2496  36046  8  43  10  64
```

61.	CO COLSPRGS	COS	21363	32337	138376	18	157	22 244
62.	CO PUEBLO	PUB	4038	10039	37436	5	34	6 54
63.	FL DAYTONA	DAB	13893	2236	82072	15	58	19 89
64.	FL FTMEYER	FMY	11304	542	45837	11	39	13 57
65.	FL PENSACOL	PNS	11205	235782	313989	11	211	13 301
66.	FL TALLAHAS	TLH	15476	8360	91952	15	53	19 82
67.	FL WESTPBEA	PBI	44938	2555	278603	37	233	45 361
68.	GA MACONROB	MCN	9482	28656	127880	5	148	7 218
69.	GA ROBINS	.	.	.	.	.	.	. .
70.	GA SAVANNAH	SAV	12316	21144	132419	12	134	14 204
71.	GU FINEGAYA	ZUA	10015	17514	36258	.	.	. .
72.	HI HILO	ITO	18253	3050	25899	21	28	26 44
73.	IA CEADRAPD	CID	13176	388	58740	18	55	26 84
74.	IA WATERLOO	ALO	9056	504	34508	12	34	15 53
75.	IL CHAMPAIG	CMI	15028	1375	73381	13	52	16 78
76.	IL ROCKFORD	RFD	9082	4067	139679	3	68	4 101
77.	IN EVANSVIL	EVV	11025	1485	77352	12	64	15 94
78.	IN FORTWAYN	FWA	18902	4571	140253	12	140	15 215
79.	IN SOUTHBND	SBN	23770	624	157670	14	164	17 241
80.	IN TERREHAU	HUF	43	3111	34411	0	33	0 50
81.	KS WICHITA	ICT	38344	14921	205917	30	223	40 336
82.	LA LAFAYETT	LFT	6132	1440	96515	7	50	8 76
83.	LA LAKECHAR	LCH	4323	1032	41260	5	24	6 37
84.	LA MONROE	MLU	8088	2351	41463	12	32	14 49
85.	MA OTIS	FMh	18644	14464	85801	.	.	. .
86.	ME BANGOR	BGR	10344	7313	53719	10	36	12 55
87.	ME PORTLAND	PWM	19859	4700	64345	12	37	15 55
88.	MI KALAMAZO	AZO	17313	2094	64019	9	56	12 81
89.	MI MUSKEGON	MKG	7708	525	35424	9	32	11 48
90.	MN DULUTH	DLH	16298	10451	44458	14	46	18 68
91.	MO SPRINGFI	SGF	12215	3445	43300	12	40	18 61
92.	MS GULFPORT	GPT	8844	18892	56080	8	43	10 64
93.	MS JACKSON	JAN	23305	11893	114869	23	75	28 112
94.	MS MERIDIAN	MEI	3131	5720	13280	4	2	4 3
95.	MT MALMSTRO	GFA	11095	12856	30900	0	39	0 52
96.	NC GREENSBO	GSO	46513	4848	240523	33	254	41 380
97.	NC WILMINGT	ILM	15424	10676	56796	11	42	13 64
98.	NH MANCHESTE	MHT	4134	906	36271	5	31	6 46
99.	NJ ATLTCITY	ACY	4796	17218	118334	5	60	33 90
100.	NV RENO	RNO	45758	4985	75650	31	56	38 87
101.	NY GRIFROME	RME	3484	25026	72000	.	62	. 91
102.	OH AKRON	CAK	11127	6607	150842	16	169	20 256
103.	OH TOLEDO	TOL	21041	3745	152495	18	155	23 237
104.	OK FORTSILL	.	.	.	.	.	.	. .
105.	OR EUGENE	EUG	9489	751	45994	10	39	12 58
106.	PA ALLENTOW	ABE	10025	1016	90016	11	59	13 90
107.	PA HARRISB	CXY	13067	7208	108560	0	122	0 167
108.	PA READING	RDG	179	596	22906	0	24	0 37
109.	PA WILKESB	AVP	9199	882	46441	7	37	8 56
110.	SC CHARLEST	CHS	20752	42520	143491	23	150	28 232
111.	SC GREENVIL	GMU	0	41	22989	18	89	22 128
112.	TN BRISTOL	TRI	19084	2294	89694	19	59	24 90
113.	TN CHATTANO	CHA	14802	3686	123092	21	134	25 208
114.	TN KNOXVILL	TYS	23620	8042	147240	29	160	36 246
115.	TX BEAUMONT	BPT	5741	926	48629	6	33	7 51
116.	TX BERGSTRO	.	.	.	.	.	.	. .
117.	TX CORPUSCH	CRP	11177	68809	123356	11	120	13 168
118.	TX FTHOOD	.	.	.	.	.	.	. .
119.	TX LONGVIEW	GGG	49	1064	35705	0	19	0 29
120.	TX LUBBOCK	LBB	20204	140808	198204	16	188	20 251

```
121.    TX WACO      ACT         41   1517  24238   0  31   0  46
122.    VA RICHMOND  RIC      32765  15631 166126  29 187  36 270
123.    VA ROANOKE   ROA      36060   3302 121477  35  86  44 128
124.    VT BURLINGO  BTV      13418  37541 137951  11 135  13 199
125.    WA FAIRCHIL     .         .      .      .   .   .   .   .
126.    WA SPOKANE   SKA      18536  14352  72220   0 145   0 207
127.    WV CLARKSBU  CKB       1988    665  38585   2  44   2  61
128.    WY CASPER    CPR       7382    323  23800  10  21  13  33
129.       ;
130.
131.    PROC SORT;
132.      BY ST SITE  YR CAR_TYP;
133.
134.    PROC PRINT;
135.      TITLE BUSY/AVERAGE RATIOS AND ANNUAL ACTIVITY LEVELS BY CARRIER TYPE;
136.      ID ST SITE YR CAR_TYP;
137.      FORMAT YR YEARF. CAR_TYP CARF.;
138.
139.    DATA TARG;  *  CONVERTS ACTIVITY LEVELS TO TARG'S;
140.      SET ACTLEV;
141.      KEEP ST SITE CODE YR  CAR_TYP  TARG_BAS;
142.
143.      IF CAR_TYP = 1 OR CAR_TYP = 2 THEN TK_FAC=.2817;
144.         ELSE TK_FAC=.3483;
145.             *   SEE PAGE A-24;
146.      TARG_BAS=ACT_LEV*(1/8760)*TK_FAC*BAR*1.2;
147.         OUTPUT;
148.
149.    PROC SUMMARY;
150.      BY ST SITE CODE YR;
151.      VAR TARG_BAS;
152.      OUTPUT OUT=TARG SUM=;
153.
154.    DATA TARG;  * EDIT PREVIOUS FILE;
155.      SET TARG;
156.      DROP _TYPE_ _FREQ_;
157.
158.    PROC PRINT;
159.      TITLE BASIC PEAK INSTANTANEOUS TARGET ESTIMATES;
160.      ID ST SITE YR ;
161.      FORMAT YR YEARF.;
162.
163.    DATA IATS;  *  CONVERTS SUMMARIZED TARG'S TO ASSOCIATED TRACKS;
164.      SET TARG;
165.      KEEP ST SITE CODE YR WTHR TARG_ADJ IAT;
166.
167.      DO K=1 TO 2;
168.        WTHR=K;
169.        WTH_FAC=.75;
170.        IF K = 2 THEN WTH_FAC=1.;
171.        TARG_ADJ=TARG_BAS*WTH_FAC;
172.        IAT=TARG_ADJ*.95;
173.        OUTPUT;
174.      END;
175.
176.    PROC SORT;
177.      BY YR WTHR IAT;
178.
179.    PROC PRINT;
180.      TITLE1 PEAK INSTANTANEOUS TARGETS ADJUSTED FOR WEATHER;
181.      TITLE2 AND ASSOCIATED TRACKS;
182.      BY YR WTHR;
183.      ID ST SITE;
184.      FORMAT YR YEARF. WTHR WTHRF.;
```

DATE
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